

BUS ARBITER  
&  
E-BUS INTERRUPT CONTROLLER  
PRELIMINARY DATA SHEET  
12 MARCH 1982

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## 1. INTRODUCTION

The SN74LS2001 BUS ARBITER is a peripheral device designed for use with the TEXAS INSTRUMENTS 9900 family, other microprocessors, and devices like DMA controllers, to provide BUS ARBITRATION for systems with multiple bus masters. The SN74LS2001 is a 20-pin, single power supply (+5V) \_\_\_\_\_ are TTL compatible device, in LS gate array technology. \_\_\_\_\_ inputs and outputs. It can also be used for the E-Bus vector interrupt control or another interrupt system using serial daisy chain and INT schemes.

## Features:

- \* Multimaster bus arbitration
- \* Synchronizes the local microprocessor with a multimaster system bus
- \* BUS TIME OUT hardware to guard against bus errors or bus dead lock
- \* E-BUS vector interrupt controller
- \* Compatible with TI's T- and E-BUS as well as many other systems  
(Like INTEL MULTI BUS, MOTOROLA VERSABUS, etc.)
- \* Compatible with TI's TMS99XXX microprocessor family and other 8 and 16 bit CPUs, like I8086, I8085, Z80, Z8000, M6800, or M68000

## 2. ARCHITECTURE

The SN74LS2001 BUS ARBITER & E-BUS INTERRUPT CONTROLLER is designed to provide low cost and high speed bus arbitration to be used with the TMS99XXX family, other microprocessors, DMA controllers, or any other system which serves as a master on a multi master system bus. The device also improves control for systems which may generate an interrupt in an E-BUS system.

Figure 1 shows the block diagram of the SN74LS2001 internal architecture. The bus arbiter consists of BUS & INTERRUPT REQUEST CONTROL, BUSY & BUS CONTROL, RELEASE CONTROL, TIMER LOGIC AND TIME OUT & READY CONTROL circuitry. In the case of an existing "BUS-REQUEST" from a master device, the BUS & INTERRUPT REQUEST CONTROL CIRCUITRY creates a system clock synchronized bus request for the following cases:

- For parallel or rotating priority bus resolving through PARALLEL BUS REQUEST (PBRQ-)
- For serial resolving through GRANTOUT
- For any request through BUS REQUEST INPUT (BRQIN-)

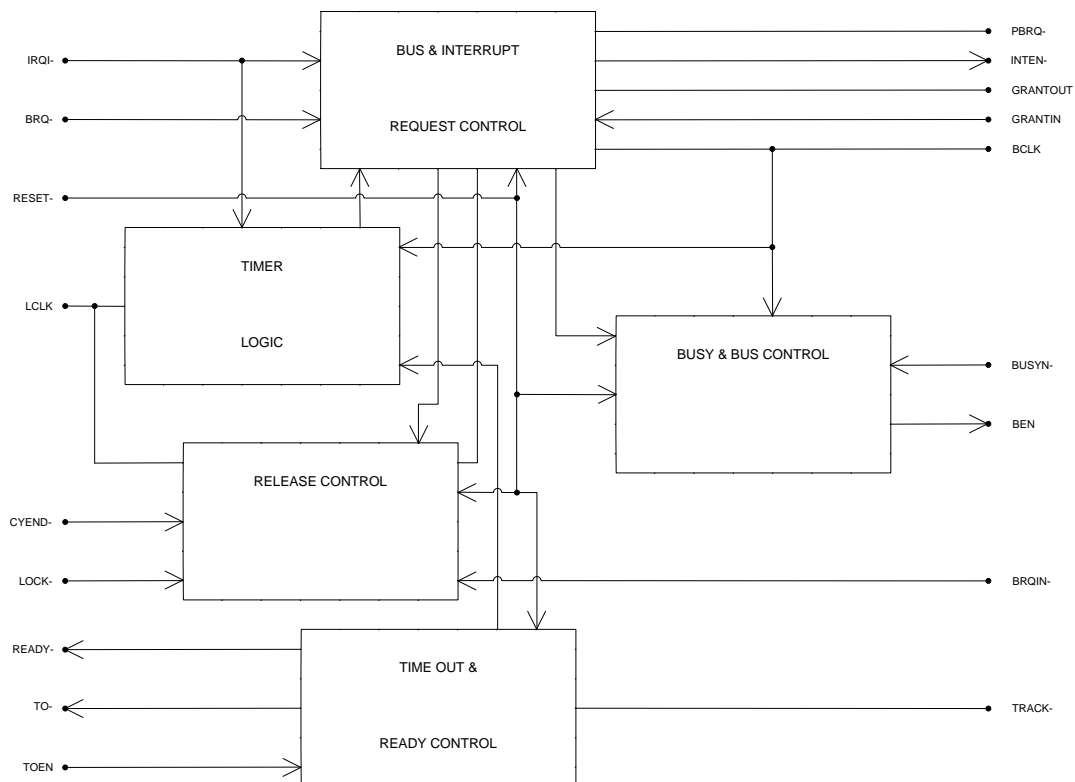


Figure 1: Block-Diagram

In interrupt mode the arbiter generates an INTERRUPT ENABLE (INTE-) signal, if an interrupt request via the INTERRUPT REQUEST INPUT (IRQI-) exists.

The BUSY & BUS CONTROL is the circuitry which monitors and activates the BUS BUSY line. It also controls the BUS ENABLE signal (BEN) which signals the local system that the bus is free for use.

The RELEASE CONTROL determines if and when the arbiter can surrender the bus.

The TIMEOUT & READY CONTROL generates the microprocessor READY signal, synchronized with the LOCAL CLOCK (LCLK), and in time-out mode, sets the BUS ERROR FLAG if an error occurs.

The TIMER LOGIC serves to create the interrupt iteration request and the TIMEOUT error logic.

### 3. FUNCTIONAL DESCRIPTION

The microprocessor issues (via address or status decoding) a BUS REQUEST (BRQ-) to the arbiter to get access to the system bus. If the microprocessor is not the current bus master, the arbiter (via BEN) inhibits the address latches, the data transceiver, and the bus control from accessing the bus and puts their outputs into high impedance. The arbiter then forces GRANTOUT and PBRQ- to a low level to indicate a request for the system bus. The arbiter monitors the bus status by checking GRANTIN (priority) and BUSYIN- (bus free) lines. During the arbitration the microprocessor is forced to a wait by an inactive READY- from the arbiter chip. In case that the arbiter finds the GRANTIN and BUSYIN- signals inactive (see appendix A fig. 1), it occupies the bus by activating BEN. Through an external bus driver (e.g., SN74LS38) BEN pulls the bus BUSY- line "low", to indicate that the bus is occupied and not available for other bus masters. BEN also enables the address latch for the data transceiver and the bus controller to access the bus. A READ operation (memory or I/O transfer can then take place. After the TRACK- signal is received from the accessed slave device, the arbiter delivers a READY signal synchronized with the local clock to the microprocessor. The microprocessor gets the READY signal and can complete its (read/write) transfer cycle.

The TIME OUT ERROR LOGIC and the INTERRUPT CONTROL will be discussed later.

4. PRIORITY RESOLVING BETWEEN BUS MASTERS

The SN74LS2001 arbiter gives the designer a great deal of flexibility to design his priority logic.

A parallel priority resolving scheme (See Fig. 2) requires a special hardware and signal wiring. Each PBRQ- output is connected to encoder/decoder logic which selects one bus master in each arbitration cycle. The bus request with the highest priority is granted by a high level on the corresponding GRANTIN line of the arbiter.

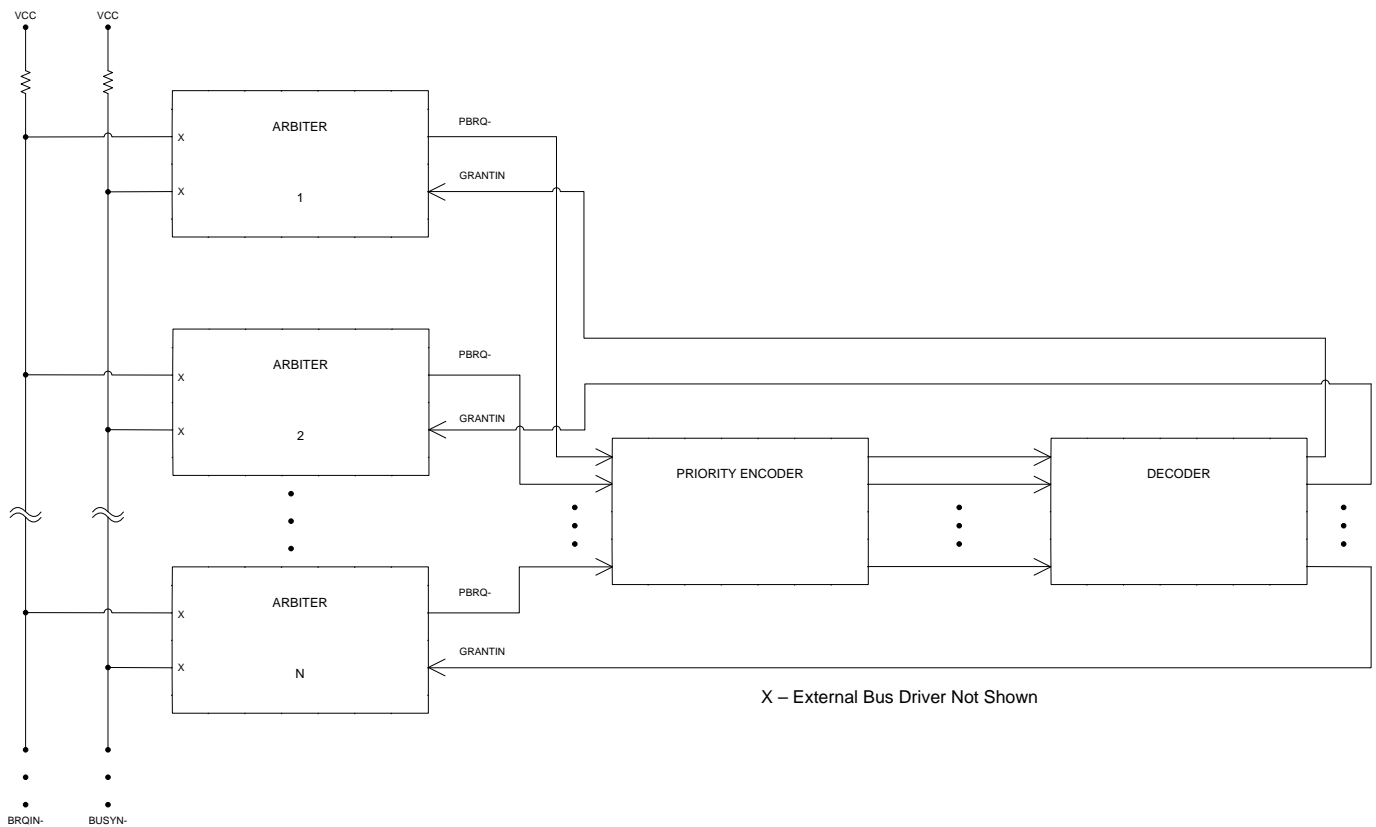


Figure 2: Parallel Priority Resolving

In serial priority resolving scheme (See Fig. 3) every higher priority GRANTOUT is connected to the next lower GRANTIN input. This type of resolving needs only an external AND-gate (e.g., 74S09) to achieve a high speed serial daisy chain.

The number of arbiters that can be used in the daisy chain loop is a function of the BUS CLOCK (BCLK) cycle and the internal processing timing of the arbiter. It can be calculated as follows:

$$\frac{T_{bclk} - (T_{sgo} + T_{sgib})}{T_{dgio}} - 1 > N$$

N = Number of arbiters in the daisy chain loop

Tsgo = Delay time from positive edge of BCLK to GRANTOUT Active (LOW)

Tsgib = Set up time, GRANTIN before positive edge of BCLK- HIGH

Tdgio = Delay time from GRANTIN to GRANTOUT of the external gate

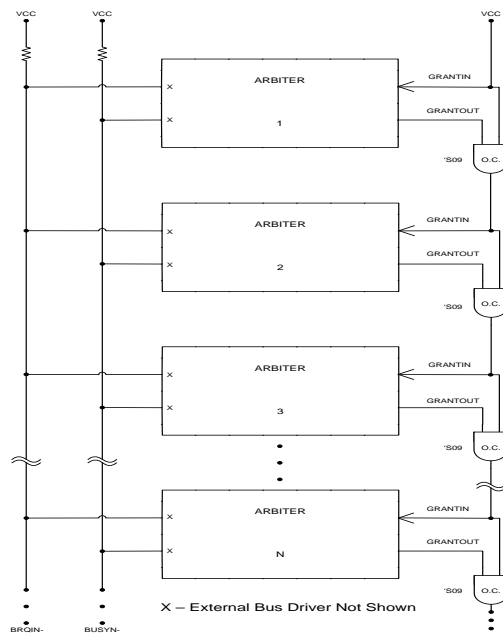


Figure 3: Serial Priority Resolving

With the SN74LS2001 device at 10mhz BCLK frequency, up to ten arbiters can be placed in the serial daisy chain.

Other priority resolving schemes (like ROUND ROBINSON, etc.), allowing a higher number of possible bus masters, can be implemented through a special priority handler & supervisor module.

The BRQIN- line can be used in the daisy chain or other resolving schemes, to signal the arbiter device that a lower priority seeks access to the bus. This allows it to keep the bus occupied if no higher or lower priority bus master is requesting access and thus reducing the synchronization time.

## 5. ARBITRATION AND SURRENDER LOGIC

Usually, when a higher priority master requests the bus, via GRANTIN, it gets the bus from a lower priority device after the lower priority device has completed its transfer cycle (See Appendix A, Fig. 2a and 2b). When it gets the bus, it will hold it if no other master is requesting the bus. A lower priority master device requests the bus from a higher priority device by pulling a BRQIN- line low. This line is normally an open collector bus line driven by the GRANTOUT output (through a non-inverted buffer) of all arbiter units in the system (wired OR). When the high priority device does not need the bus (See Appendix A, Fig 2c), it releases it, so that the lower priority device can gain access to it. A summary of the conditions under which the arbiter will release the bus on the negative edge of LCLK, is given by the following functions:

$BRQ- = \text{LOW}, GRANTIN = \text{LOW}, CYEND = \text{LOW}, LOCK- = \text{HIGH}$

(See Appendix A, Fig. 2a)

$BRQ- = \text{HIGH} \ \& \ GRANTIN = \text{LOW} \ \& \ LOCK- = \text{HIGH}$

(See Appendix A, Fig. 2b)

$BRQ- = \text{HIGH} \ \& \ BRQIN- = \text{LOW} \ \& \ LOCK- = \text{HIGH}$

(See Appendix A, Fig. 2c)

## 6. LOCK LOGIC

The arbiter LOCK- input provides a possibility for the microprocessor to inhibit a bus release regardless of whether the bus is requested by any other bus master or not. If the microprocessor executes a non interruptible instruction sequence, like a semaphore test, it sets the LOCK- input of the arbiter to a LOW level. This ensures that the bus is not surrendered during multiple bus transfers, even if the BRQ- input becomes inactive between two bus transfers. LOCK also disables the interrupt cycle generated through IRQI-. The system designer must ensure that the LOCK function is used properly and not result in a bus dead lock situation.



## 7. BUS ANTI DEAD LOCK SYSTEM

The arbiter has the ability to identify and indicate a bus time-out error. There are two kinds of error that can be recognized (See Appendix A, Fig. 3). The first one (To1), occurs when the microprocessor desires the bus and the bus is busy for more than 128 BCLK cycles. This kind of notification gives the microprocessor the opportunity to start an error recovery routine and identify bus dead hardware malfunction.

The second type of time out error (To2) appears when the local microprocessor is the current bus master, executing a bus transfer to a slave module, does not get a TRACK- signal back within 16 LCLK cycles. This kind of error gives the microprocessor the opportunity to continue operation even if an erroneous or not existing slave has been addressed by the software. To recognize which type of error exists (To1 or To2), the BEN signal has to be latched with the negative going edge of the TIME OUT (TO) error flag. If the BEN signal is inactive, To1 occurred; otherwise To2 caused the bus error.

In case of error, the arbiter activates READY- and allows that the microprocessor can complete the current instruction and accept the TO flag.

The TOEN is the signal that enables (HIGH) the time out error circuitry. When LOW, it resets the TO signal and disables the logic.

## 8. INTERRUPT CONTROL LOGIC

The arbiter can operate in an E-BUS interrupt mode as well. When an interrupt source wants to send a vector interrupt it activates (LOW) the interrupt request input (IRQI-). The arbiter drives the GRANTOUT to LOW and waits for the bus to be free via GRANTIN and BUSYN- (See Appendix A, Fig. 4). If it finds the bus free it generates for one BCLK cycle an interrupt enable (INTE-) signal. This signal serves also to activate the buffer, which puts the interrupt vector onto the E-BUS. If there is no response from the microprocessor which handles the interrupt, the vector is sent again after a 128 BCLK as long as the IRQI- input is active.

The interrupt arbitration request through IRQI- has a higher on-chip priority than the BRQ- request. This means that the arbiter will inhibit a bus transfer (BEN goes LOW) at the end of a cycle (CYEND = LOW) for one BCLK cycle to issue an interrupt if no higher priority device is requesting the bus and the LOCK- input is inactive (See also Appendix A, Fig. 4).

9. SYSTEM CONFIGURATIONS

Some applications of the SN74LS2001 Bus Arbiter/E-Bus Interrupt Controller are presented in Appendix B.

10. PIN ASSIGNMENTS

Figure 4 shows the arbiter 20 pin DIL package. All signals are described on the following pages.

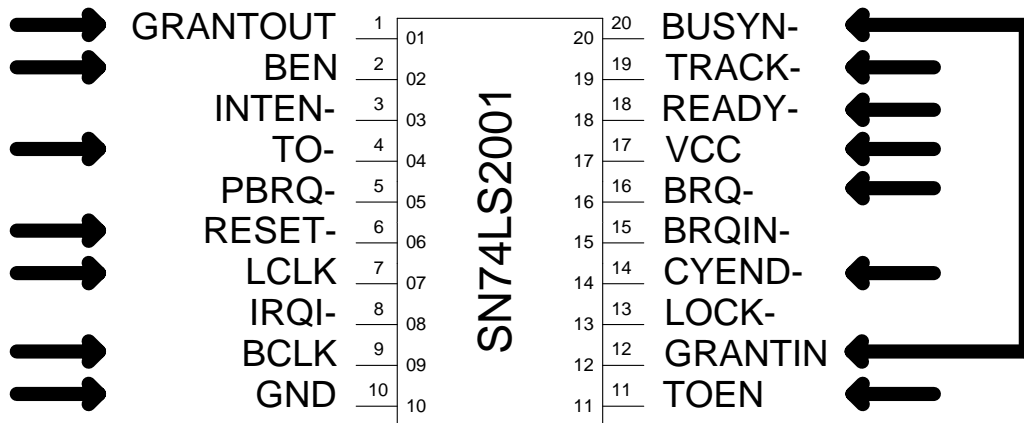


Figure 4: 20 pin dual in line package

NOTE: Pins identified with arrows are used by the Powertran Cortex computer. Pins connected by a pair of arrows are used in an opposite fashion to their descriptions as implemented by the Powertran Cortex.

<u>SIGNATURE</u>	<u>I/O</u>	<u>DESCRIPTION</u>
RESET-	IN	RESET: RESET- is an active LOW signal input which is used to RESET/Initialize the arbiter. After RESET no arbiter has the bus and all output signals are inactive.
LCLK	IN	LOCAL CLOCK: This is the on board clock which serves to synchronize the release logic so that the bus can be surrendered with proper timing. It is also used as the time out clock and to synchronize READY-.
BCLK	IN	BUS CLOCK: The multi master system clock which synchronizes bus arbitration.
BRQ-	IN	BUS REQUEST: BRQ- is an active LOW input signal which tells the arbiter to request the bus by pulling GRANTOUT LOW and activating PBREQ-, and to occupy it as long as no higher priority bus master request is received.
IRQI-	IN	INTERRUPT REQUEST IN: This input is an active LOW signal, which serves to generate an E-BUS interrupt cycle every 128 BCLK cycles as long as IRQI- stays active.
PBRQ-	OUT	PARALLEL BUS REQUEST: This active LOW output serves as a parallel bus request and is activated by the arbiter to indicate an access request. It will stay active as long as BRQ- is active, an interrupt cycle is pending, and the arbiter is not the current bus master.
INTE-	IN	INTERRUPT ENABLE: INTE- is driven active LOW for one BCLK cycle if the arbiter has the bus and is generating an E-BUS interrupt cycle.
BRQIN-	IN	BUS REQUEST INPUT: BRQIN- is an input signal to the arbiter which serves to indicate if a lower priority master is requesting access to the bus.  The BRQIN- is connected to a bidirectional bus line driven by the GRANTOUT signal of all arbiters in the system.  If the BRQIN- input is active and the arbiter is the current bus master without an active bus request through BRQ- or IRQI- it will release the bus to the lower priority master.

<u>SIGNATURE</u>	<u>I/O</u>	<u>DESCRIPTION</u>
GRANTIN	IN	ACCESS GRANT IN: This is an input signal that, when HIGH, indicates to a potential bus master that no higher priority bus master device requires access to the bus, and consequently allows it to vie for control of the bus.
GRANTOUT	OUT	ACCESS GRANT OUT: When HIGH, it indicates that lower priority bus masters may vie for control of the bus. This signal is used in the serial priority resolving scheme. The GRANTOUT pin of one slot is always connected to the GRANTIN pin of the next slot with lower positional priority. GRANTOUT will go active (LOW), synchronized with BCLK, after a bus or interrupt request has arrived. It will go inactive, when the device has acquired the bus.
LOCK-	IN	LOCK: LOCK- is an active LOW input signal used to inhibit the arbiter from surrendering the bus to any other bus master requesting bus access (regardless of priority). It will also inhibit any interrupt cycle request through IRQI-.
BEN	OUT	BUS ENABLE: BEN is an active HIGH output and serves to signal a bus controller, the bus transceiver, and any other devices, that the system bus can be connected to the local bus. BEN is also used to drive the BUSY- bus line through an open collector bus driver (active LOW) to indicate to all other possible bus masters that the bus is occupied
BUSYN-	IN	BUSY IN: BUSYN- is an active LOW input from the system bus and indicates that the bus is currently used by another bus master. A HIGH level on BUSYN- and GRANTIN signals the arbiter that the bus is not used and can be occupied after the LOW to HIGH transition of BCLK.
TRACK-	IN	TRANSFER ACKNOWLEDGE: TRACK- is an input signal, when active (LOW), indicates that an addressed slave device is ready to complete its read or write operation. This signal is synchronized with the raising edge of LCLK and fed to the READY- output.

<u>SIGNATURE</u>	<u>I/O</u>	<u>DESCRIPTION</u>
READY-	OUT	READY: READY- is an output signal which, when active (LOW), indicates to the microprocessor that it can complete its read or write operation. READY- is synchronized to the LCLK. READY- is the same as the TRACK- signal on normal operation. It will be internally created in the time out mode (TOEN = HIGH) when a TIME OUT error is detected.
CYEND-	IN	CYCLE END: CYEND- is a signal generated by the microprocessor which, when active (LOW), allows the arbiter to surrender the bus if a higher priority master requests the bus via GRANTIN.
TO-	OUT	TIME OUT: TO- is an active LOW output signal which is used to flag the microprocessor that a time out error is detected on the bus. The signal is generated only when TOEN is active.
TOEN	IN	<p>TIME OUT ENABLE: TOEN is an input signal (active HIGH) which enables the TIME OUT CONDITION DETECTION scheme to create a TO flag and READY- signal in two cases:</p> <p>a) When the arbiter does not get the bus for 128 BCLK cycles.</p> <p>b) When the arbiter has acquired the multi master bus, an input or output operation has been initiated, and no response is received after 16 LCLK cycles from the addressed slave device.</p> <p>This scheme is a guard against bus errors and bus dead locks. When TOEN does go LOW, it also clears the TO error flag and disables the time out logic.</p>
VCC	IN	Supply voltage +5 volts DC +/-5%.
GND	IN	GROUND.

## 11. ELECTRICAL SPECIFICATIONS

## 11.1 RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
Supply Voltage, $V_{CC}$	4.75	5	5.25	V
Supply Voltage, $V_{SS}$		0		V
High-Level Input Voltage, $V_{IH}$	2			V
Low-Level Input Voltage, $V_{IL}$			0.8	V
Operating Free-Air Temperature, $T_A$		0	70	$^{\circ}C$

## 11.2 ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	TYPE
$I_I$ Input current at max input voltage	$V_{CC} = \text{max}, V_{IH} = 7V$			0.1	$\mu A$
$I_{OL}$ Low-level output current					
READY- signal *	$V_{OL} = 0.5V$			16	mA
GRANTOUT signal	$V_{OL} = 0.4V$			8	mA
PBRQ- signal	$V_{OL} = 0.5V$			8	mA
INTE- signal	$V_{OL} = 0.4V$			8	mA
BEN signal	$V_{OL} = 0.4V$			8	mA
TO- signal	$V_{OL} = 0.4V$			8	mA
$I_{OH}$ High-level output current *	$V_{OH} = 2.7V$			*-400	$\mu A$
$I_{OH}$ High-level output current	$V_{OH} = 2.7V$			-250	$\mu A$
$I_{IH}$ High-level input current	$V_{CC} = \text{max}, V_{IH} = 2.7V$			20	$\mu A$
$I_{IL}$ Low-level input current, GRANTIN	$V_{CC} = \text{max}, V_{IL} = 0.5V$			-0.4	mA
$I_{IL}$ Low-level input current, all others	$V_{CC} = \text{max}, V_{IL} = 0.5V$			-0.2	mA
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{min}, V_{IH} = 2V$ $V_{IL} = V_{IL} \text{ max}$	$I_{OL} = 8 \text{ mA}$		0.4	V
		$I_{OL} = 16 \text{ mA}$		0.5	v
$V_{OH}$ High-level output voltage	$V_{CC} = \text{min}, V_{IH} = 2V$ $V_{IL} = V_{IL} \text{ max}, I_{OH} = -400 \mu A$	2.7	3.4		V
$I_{CC}$ Supply current	$V_{CC} = \text{max}$		60		mA

\* Open collector output with 10K ohm pull up

## 11.3 TIMING REQUIREMENTS OVER FULL RANGE OF OPERATING CONDITIONS

PARAMETER		MIN	TYP	MAX	UNIT
$T_{BCLK}$	Bus clock cycle time	100	250		ns
$T_{BCLK R}$	Bus clock rise time		10	15	ns
$T_{BCLK F}$	Bus clock fall time		10	15	ns
$T_{BCLK W(L)}$	Bus clock pulse width (low-level)	50	125		ns
$T_{BCLK W(H)}$	Bus clock pulse width (high-level)	50	125		ns
$T_{LCLK}$	Local clock cycle time	100	250		ns
$T_{LCLK R}$	Local clock rise time		8	10	ns
$T_{LCLK F}$	Local clock fall time		8	10	ns
$T_{LCLK W(L)}$	Local clock pulse width (low-level)	50	125		ns
$T_{LCLK W(H)}$	Local clock pulse width (high-level)	50	125		ns
$T_R W(L)$	Reset pulse width (low-level)		50		ns

## 11.4 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	TYP*	MAX*	UNIT
$T_{SB}$	Setup time BUSYN- before BCLK $\uparrow$		15	20	ns
$T_{HB}$	Hold time BUSYN- after BCLK $\uparrow$	0	20		ns
$T_{dBEH}$	Delay time BEN (high) after BCLK $\uparrow$		10		ns
$T_{dBEL}$	Delay time for BEN after LCLK $\downarrow$		10		ns
$T_{dGO}$	Delay time GRANTOUT after BCLK $\uparrow$	0	10		ns
$T_{SBRIN}$	Setup time BRQIN-		20		ns
$T_{HBRIN}$	Hold time in BRQIN-	0			ns
$T_{dPBRL}$	Delay time PBRQ- (low) after BCLK $\uparrow$		20		ns
$T_{dPBRH}$	Delay time PBRQ- (high) after LCLK		20		ns
$T_{dIT}$	Delay time INTE- after BCLK $\uparrow$		10		ns
$T_{SGI}$	Setup time GRANTIN before BCLK $\uparrow$		10		ns
$T_{HGI}$	Hold time GRANTIN after BCLK $\uparrow$	0			ns
$T_{STR}$	Setup time TRACK- before LCLK $\uparrow$		10		ns
$T_{dRH}$	Delay time READY- (high) after CYEND- (low)		20		ns
$T_{dTRH}$	Delay time READY- (low) after LCLK $\uparrow$		15		ns
$T_{dTOL}$	Delay time TO- (low) after LCLK $\uparrow$		20		ns
$T_{dTOH}$	Delay time TO- (high) after TOEN (low)		20		ns

\* Design goals

APPENDIX A: TIMING DIAGRAMS



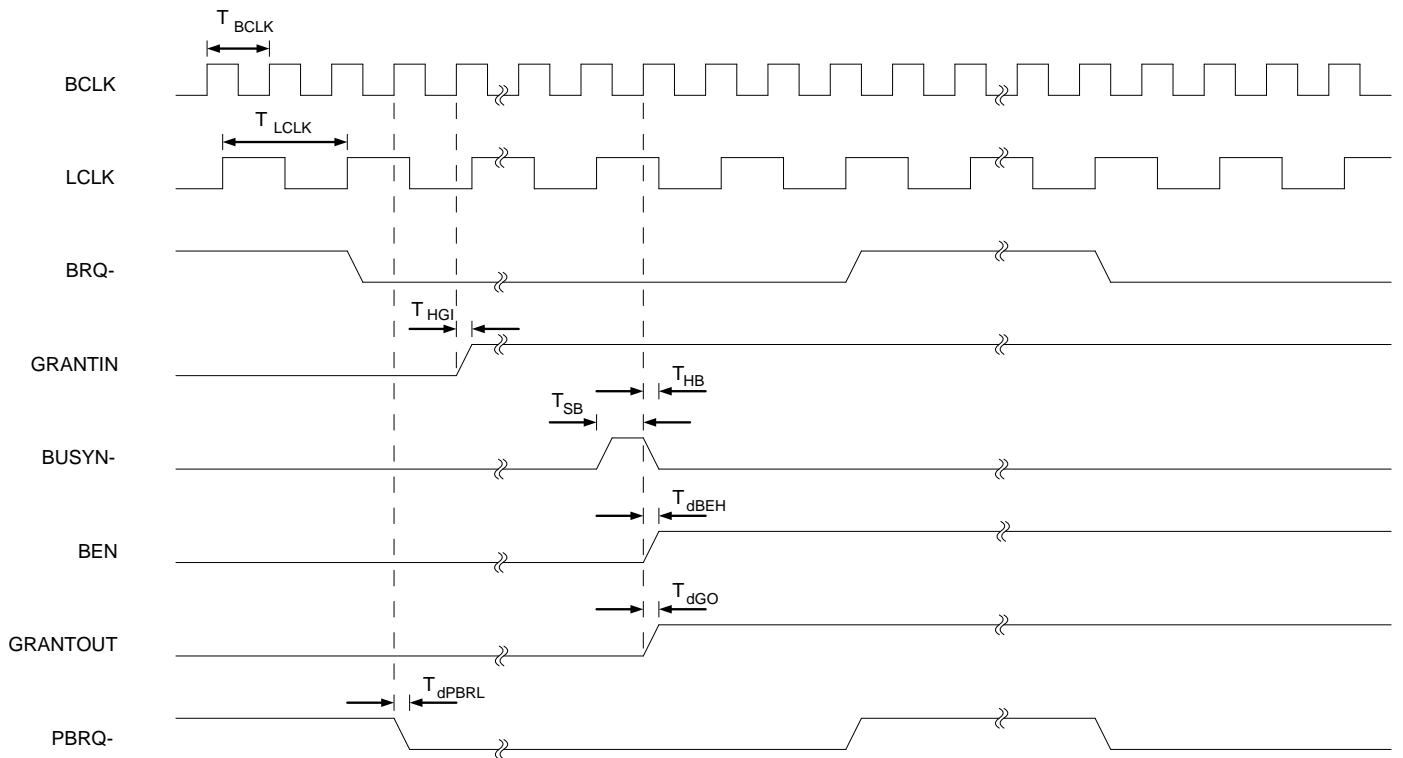


Figure 1: Bus Requests

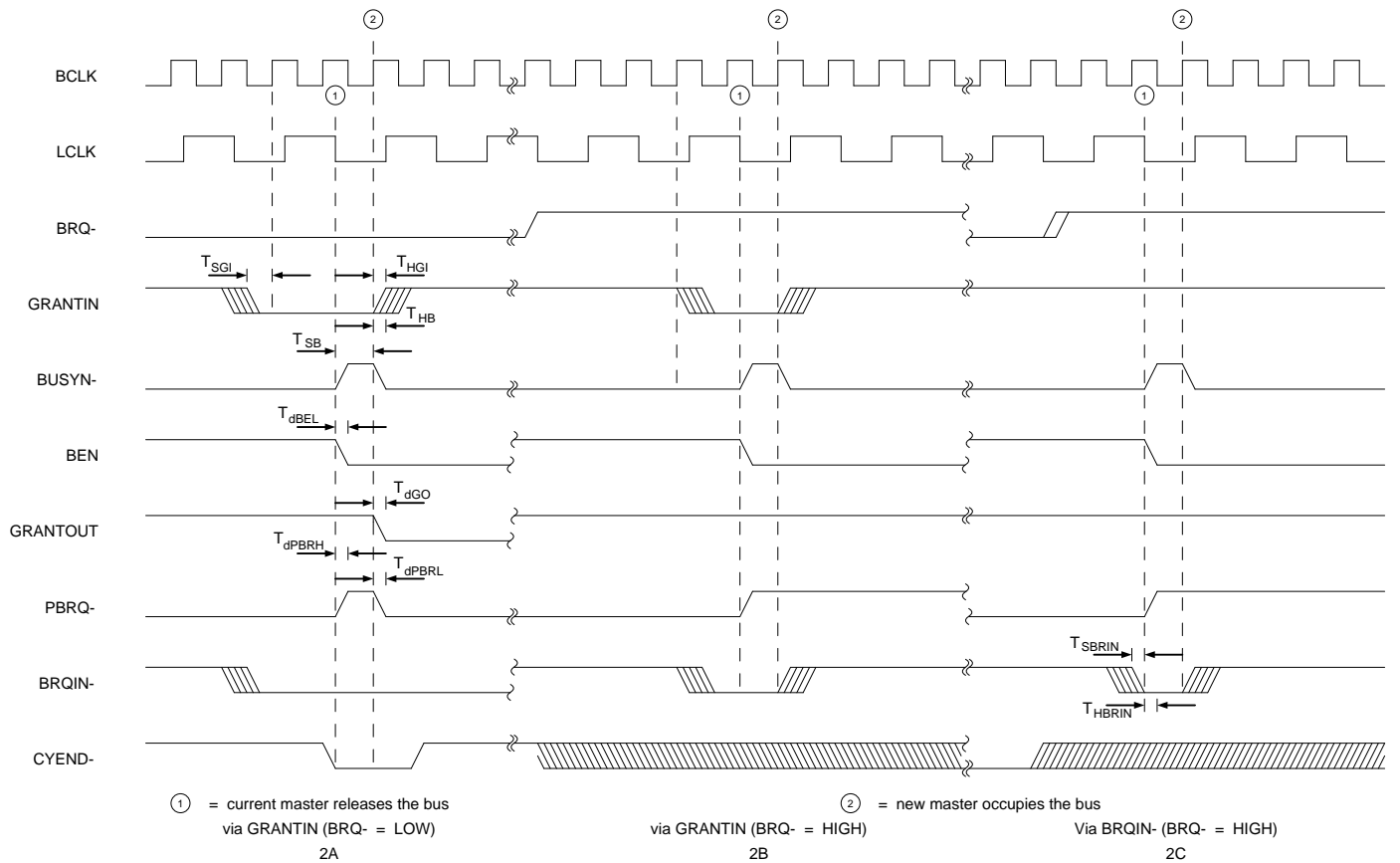


Figure 2: Bus Surrendering

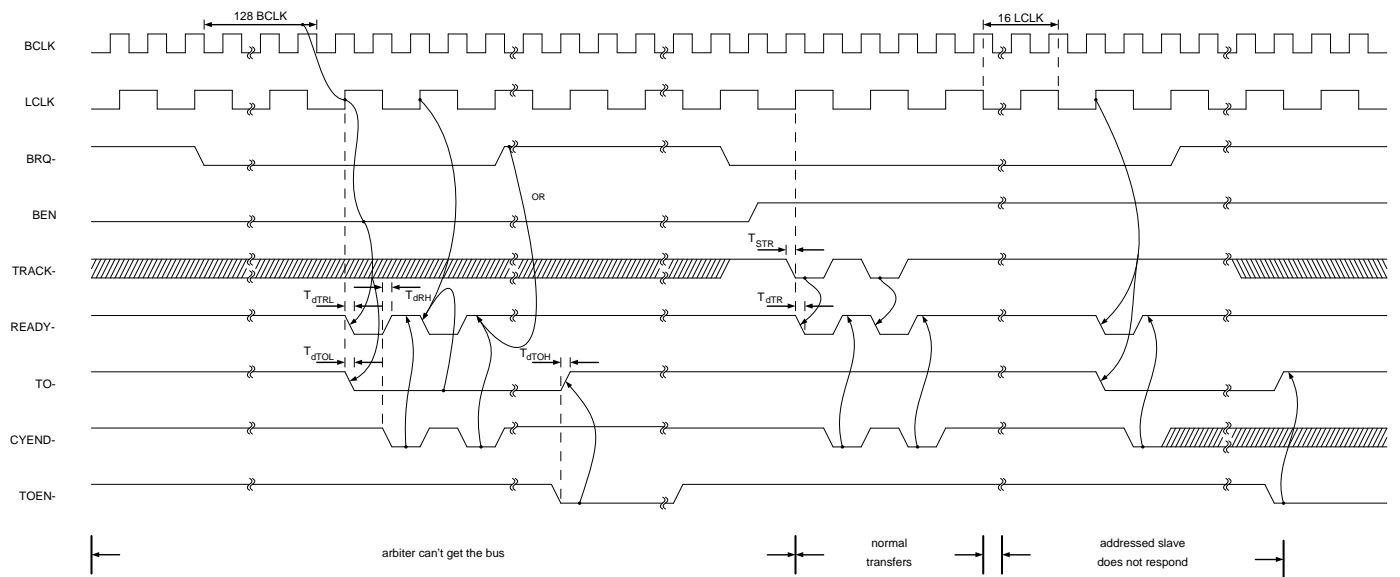


Figure 3: Ready & Bus Anti Dead Lock Logic

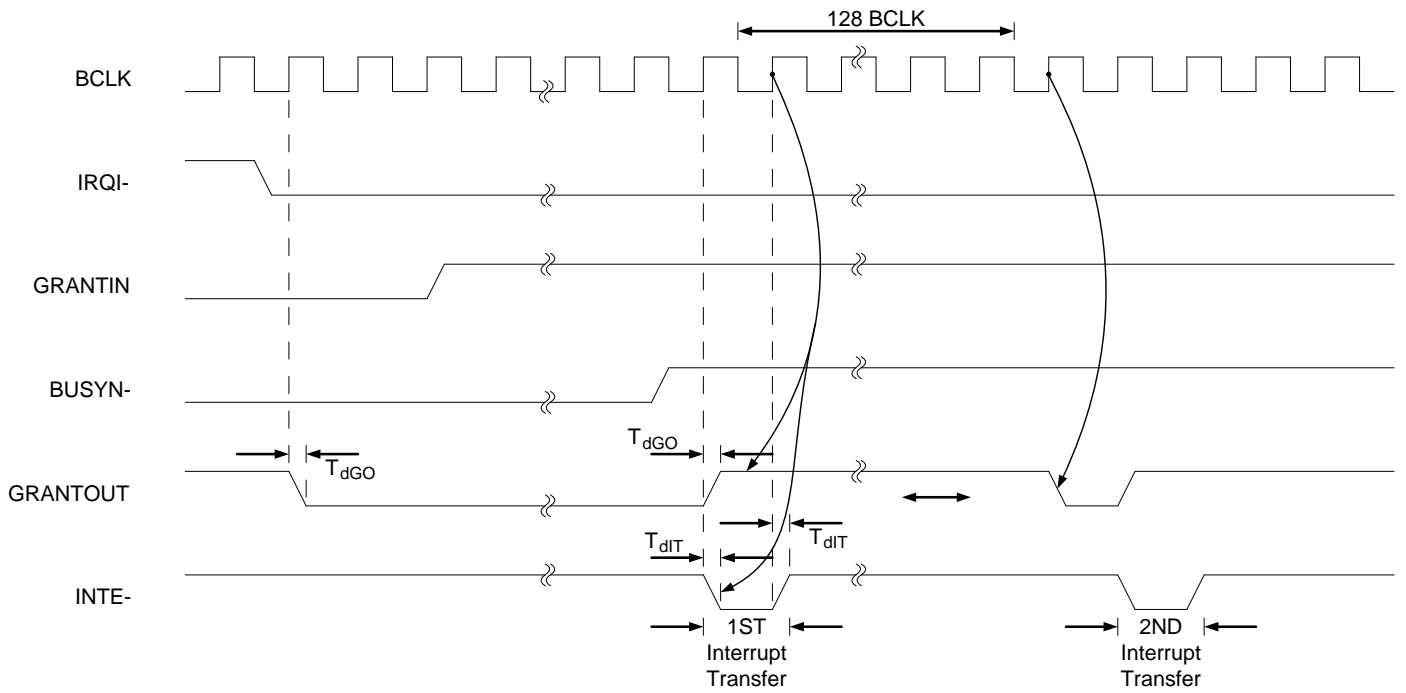


Figure 4: Interrupt Timing

APPENDIX B: SYSTEM CONFIGURATION BLOCK DIAGRAMS

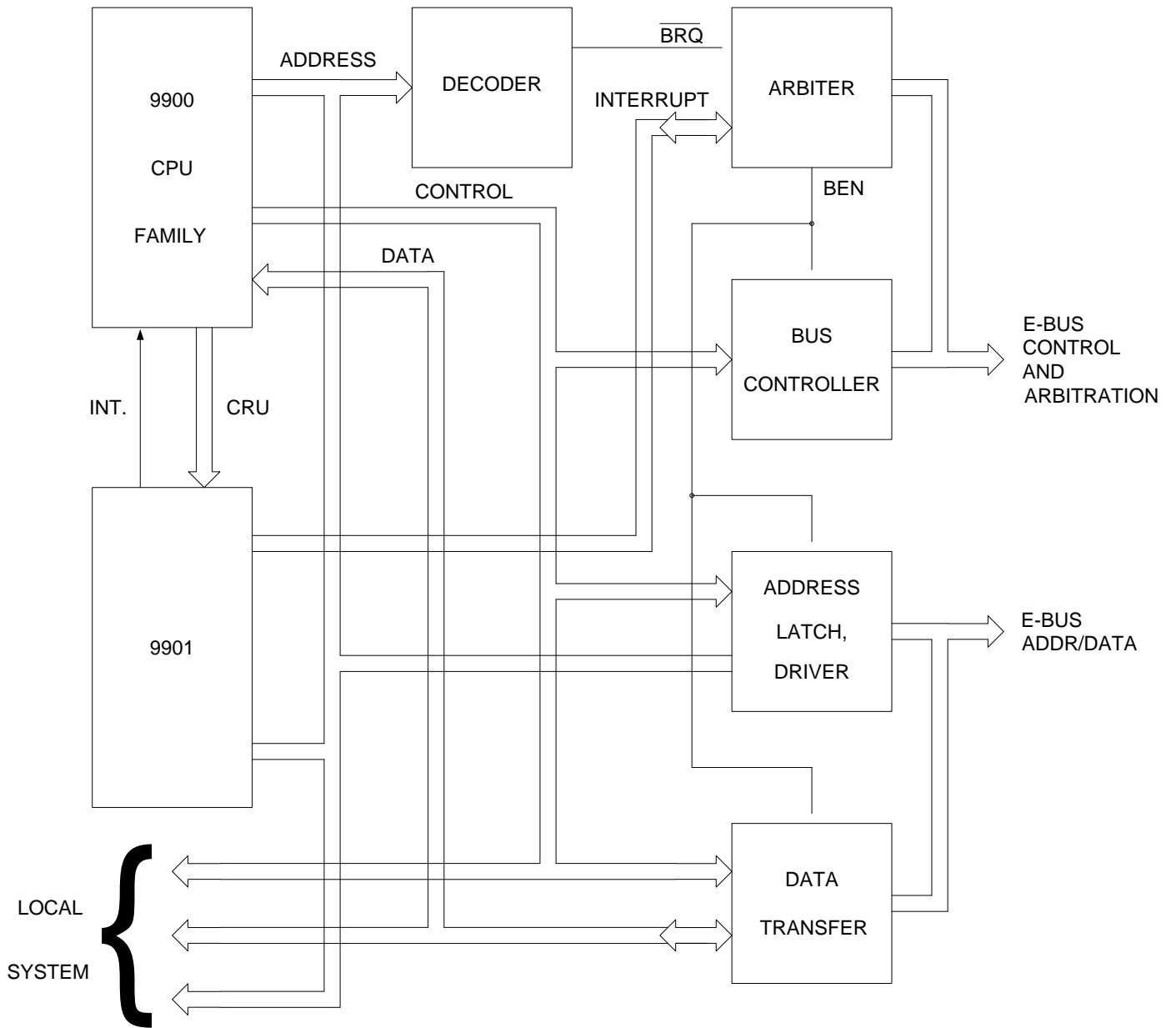


Figure 1: 99XXX Family Multiprocessing

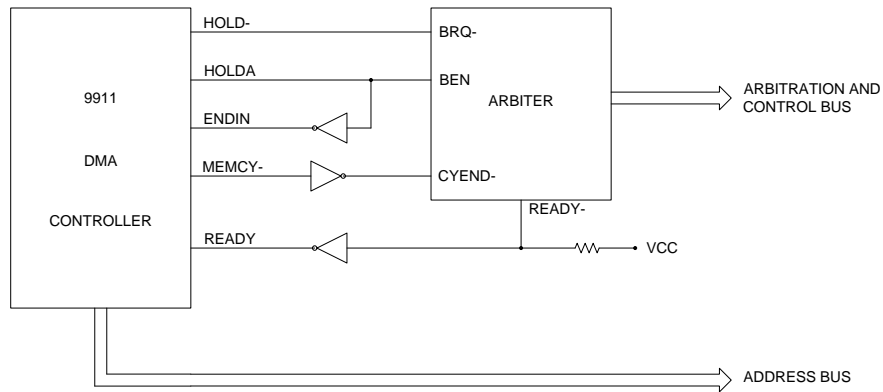


Figure 2: Multiprocessing with TMS 9911 DMA-Controller

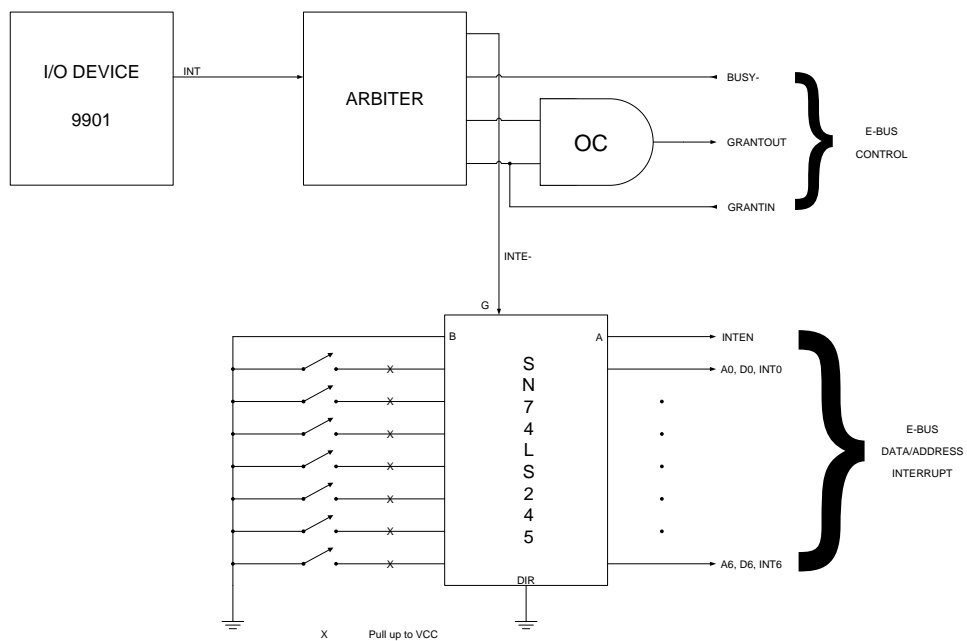


Figure 3: Interrupt Control

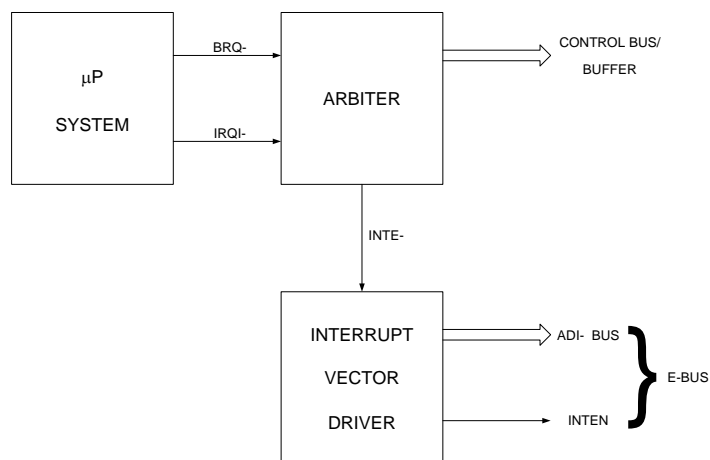


Figure 4: Bus Arbitration & Interrupt Control

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