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BUS ARBITER
&
E-BUS INTERRUPT CONTROLLER
PRELIMINARY DATA SHEET
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1 INTRODUCTION.

The SN74LSXXX BUS ARBITER is a peripheral device designed for use the TEXAS INSTRUMENTS 9900 family, other microprocessors, and dev like DMA controller, to provide BUS ARBITRATION for systems with mult bus masters. The SN74LSXXX is a 20 pin, single power supply (+5V are TTL compatible compatible device, in LS gate array technology. inputs and outputs. It can also be used for the E-BUS vector inter control or another interrupt system using serial daisy chain and IN schemes.

Features:

* Multimaster bus arbitration.

* Sychronizes the local microprocessor with a multi master system bus.

* BUS TIME OUT hardware to guard against bus errors or bus dead lock.

* E-BUS vector interrupt controller.

* Compatible with TI's T- and E-BUS as well many other systems (like INTEL MULTI BUS, MOTOROLA VERSABUS, etc.).

* Compatible with TI's TMS99XXX microprocessor family and other 8 and 16 bit CPU's, like I8086, I8085, Z80, Z8000, M6800 or M68000.

2 ARCHITECTURE.

The SN74LSXXX BUS ARBITER & E-BUS INTERRUPT CONTROLLER is design provide low cost and high speed bus arbitration to be used with TMS99XXX family, other microprocessors, DMA controllers, or any o system which serves as a master on a multi master system bus. device also improves control for systems which may generate an inter in an E-BUS system.

Figure 1 shows the block diagram of the SN74LSXXX internal architect The bus arbiter consists of BUS & INTERRUPT REQUEST CONTROL, BUSY & CONTROL, RELEASE CONTROL, TIMER LOGIC AND TIME OUT & READY CON circuitry. In the case of an existing "BUS-REQUEST" from a ma device, the BUS & INTERRUPT REQUEST CONTROL CIRCUITRY creates a sy clock synchronized bus request for the following cases:

- for parallel or rotating priority resolving through PARALLEL BUS REQUEST (PBRQ-).
- for serial resolving through GRANTOUT.
- for any request through BUS REQUEST INPUT (BRQIN-).

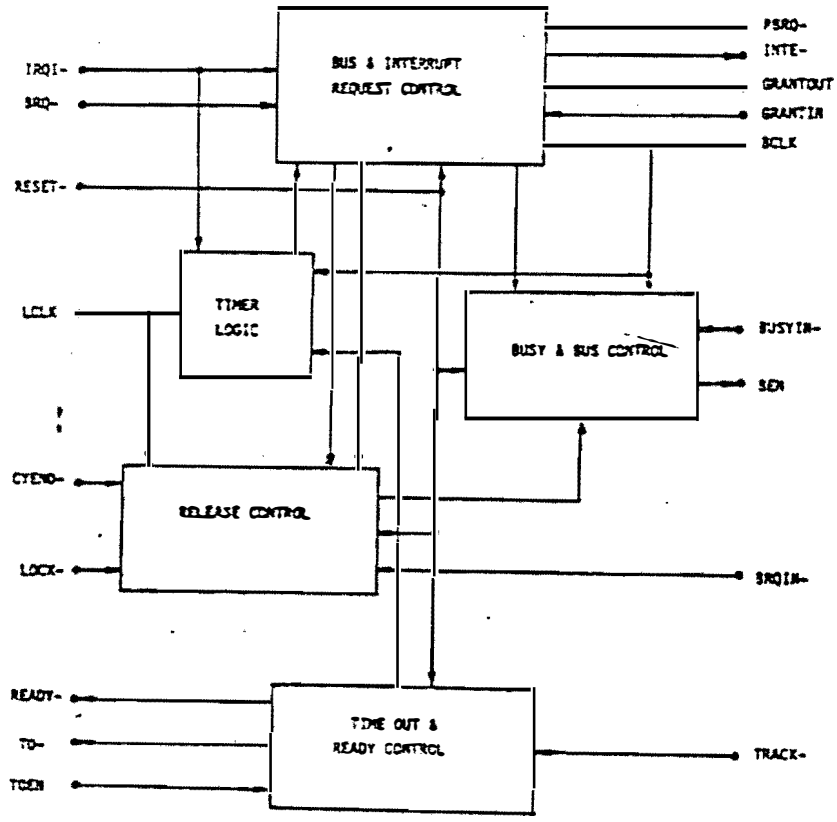

Figure 1: Block-Diagram

In interrupt mode the arbiter generates an INTERRUPT ENABLE (INT signal, if an interrupt request via the INTERRUPT REQEST INPUT (IRQ exists.
The BUSY & BUS CONTROL is the circuitry which monitors and activates bus BUSY LINE. It also controls the BUS ENABLE (BEN) signal wh signals the local system that the bus is free for use.
The RELEASE CONTROL determines if and when the arbiter can surrender bus.
The TIMEOUT & READY CONTROL generates the microprocessor READY sig syncronized with the local clock (LCLK), and in time-out mode, sets BUS ERROR FLAG if an error occurs.
The TIMER LOGIC serves to create the interrupt iteration request and TIMEOUT error logic.

3 FUNCTIONAL DESCRIPTION.

The microprocessor issues (via address or status decoding) a BUS REQU (BRQ-) to the arbiter to get access to the system bus. If microprocessor is not the current bus master, the arbiter (via B inhibits the address latches, the data transceiver and the bus control from accessing the bus and puts their outputs into high impedence. arbiter then forces GRANTOUT and PBRQ- to a low level to indicat request for the system bus. The arbiter monitors the bus status checking GRANTIN (priority) and BUSYIN- (bus free) lines. During arbitration the microprocessor is forced to a wait by an inactive REA from the arbiter chip. In case that the arbiter finds the GRANTIN BUSYIN- signals inactive (see appendix A fig. 1), it occupies the bus activating BEN. Through an external bus driver (e.g SN74S38) BEN pu the bus BUSY- line "low", to indicate that the bus is occupied and available for other bus masters. BEN also enables the address latch the data transceiver and the bus controller to access the bus. A operation (memory or I/O transfer) can then take place. After the TRA signal is recieved from the accessed slave device, the arbiter deliver Ready Signal synchronised with the local clock to the microprocessor microprocessor gets the ready signal, and can complete its (read write) transfer cycle.
The time out error logic and the interrupt control will be discus later.

4 PRIORITY RESOLVING BETWEEN BUS MASTERS.

The SN74LSXXX arbiter gives the designer a great degree of flexibility design his priority logic.
A parallel priority resolving scheme (see fig. 2) requires a spec hardware and signal wiring. Each PBRQ- output is connected to encoder/decoder logic which selects one bus master in each arbitrat cycle. The bus request with the highest priority is granted by a h level on the corresponding GRANTIN line of the arbiter.

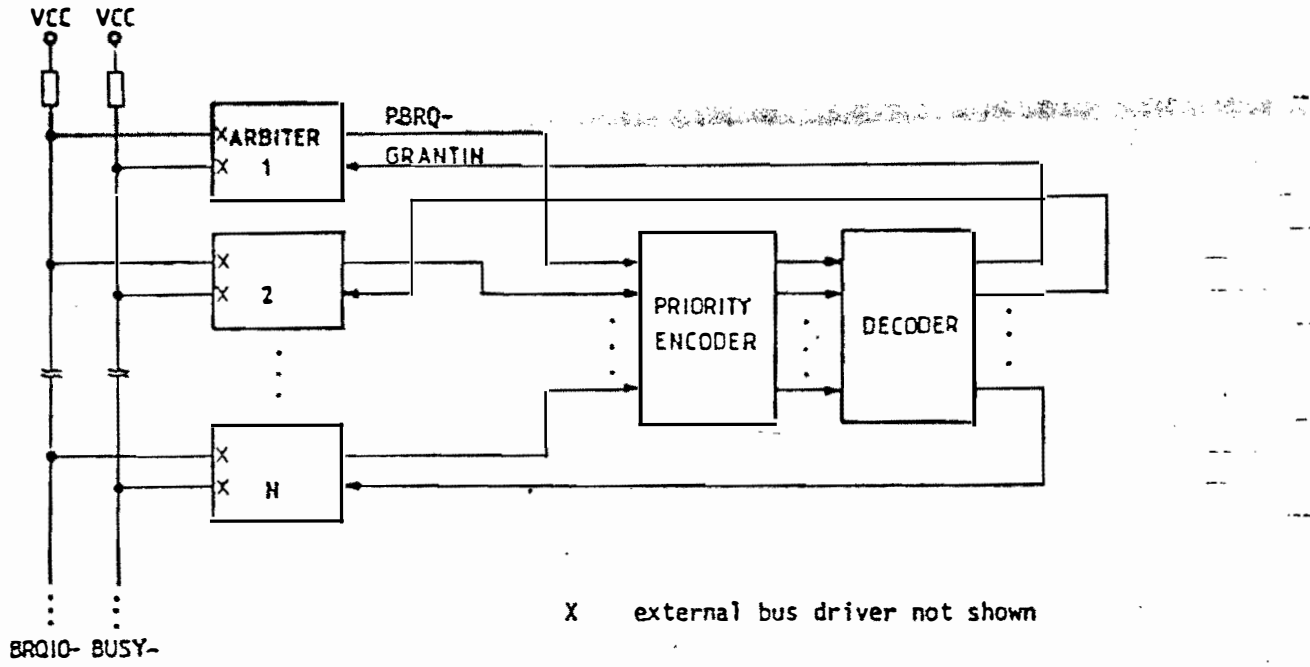

Figure 2: Parallel Priority Resolving

In serial priority resolving scheme (see fig. 3) every higher prior GRANTOUT is connected to the next lower priority GRANTIN input. T type of resolving needs only an external AND-gate (e.g. SN74S09) achieve a high speed serial daisy chain.

...e number of arbiters that can be used in the daisy chain loop i... function of the BUS CLOCK (BCLK) cycle time and the internal proces... timing of the arbiter. It can be calculated as follows:

$$\frac{Tbclk - (Tsgo + Tsgib)}{Tdgio} - 1 > N$$

N = Number of arbiters in the daisy chain loop.

Tsgo = Delay time from positive edge of BCLK to GRANTOUT active (LOW).

Tsgib = Set up time, GRANTIN before positive edge of BCLK- HIGH.

Tdgio = Delay time from GRANTIN to GRANTOUT of the external gate.

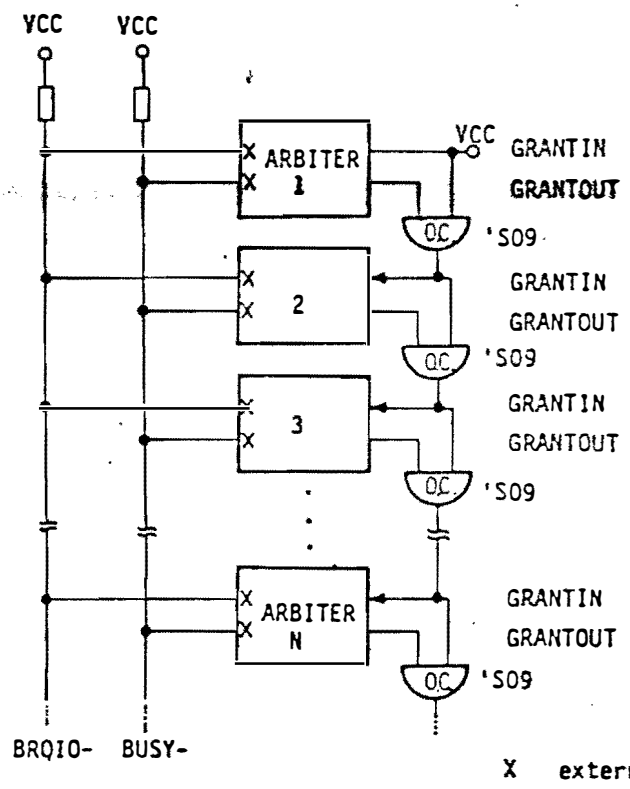

Figure 3: Serial Priority Resolving

With the SN74LSXXX device at 10mhz BCLK frequency, up to 10 arbiters be placed in the serial daisy chain.
Other priority resolving schemes (like ROUND ROBINSON, ect.), a higher number of possible bus masters, can be implemented throug special priority handler & supervisor module.
The BRQIN- line can be used in the daisy chain or other resol schemes, to signal the arbiter device that a lower priority seeks ac to the bus. This allows to keep the bus occupied if no higher or l priority bus master is requesting access and thus reducing synchronisation time.

5 ARBITATION AND SURRENDER LOGIC.

Usually, when a higher priority master requests the bus, via GRANTIN gets the bus from a lower priority device after the lower priority de has completed its transfer cycle (see appendix A, fig. 2a and 2b). it gets the bus, it will hold it if no other master is regesting the A lower priority master device requests the bus from a higher pric device by pulling a BRQIN- line low. This line is normally an collector bus line driven by the GRANTOUT output (through a non-inver buffer) of all arbiter units in the system (wired OR). When the hi priority device does not need the bus (see appendix A, fig. 2c releases it, so that the lower priority device can gain access to it. A summary of the conditions under which the arbiter will release the on the negative edge of LCLK, is given by the follwing functions:

BRQ- = LOW, GRANTIN = LOW, CYEND = LOW, LOCK- = HIGH

(see appendix A figure 2a)

BRQ- = HIGH & GRANTIN = LOW & LOCK- = HIGH

(see appendix A figure 2b)

BRQ- = HIGH & BRQIN- = LOW & LOCK- = HIGH

(see appendix A figure 2c)

6 LOCK LOGIC.

The arbiter LOCK- input provides a possibility for the microprocesso inhibit a bus release regardless whether the bus is requested by other bus master or not. If the microprocessor executes a interruptable instruction sequence, like a semaphore test, it sets LOCK-. input of the arbiter to a LOW level. This ensures that the bu not surrendered during multiple bus transfers, even if the BRQ- i becomes inactive between two bus transfers. LOCK also disables interrupt cycle generated through IRQI-. The system designer must en that the LOCK function is used properly and not result in a bus dead situation.

7 BUS ANTI DEAD LOCK SYSTEM.

The arbiter has the ability to identify and indicate a bus time-ou error. There are two kinds of error that can be recognized (see appendi A fig. 3). The first one (To1), when the microprocessor desires the bu and the bus is busy for more then 128 BCLK cycles. This kind o notification gives the microprocessor the opportunity to start an erro recovery routine and identify bus dead
hardware malfunction.

The second type of time out error (To2) appears when the loca microprocessor is the current bus master, executing a bus transfer to slave module, does not get a TRACK- signal back within 16 LCLK cycles This kind of error gives the microprocessor the opportunity to continu operation even if an errornous or not existing slave has been addresse by the software. To recognise which kind of error exists (To1 or To2) the BEN signal has to be latched with the negative going edge of th TIME-OUT (TO) error flag. If the BEN signal is inactive. To1 occured otherwise To2 caused the bus error.
In case of error, the arbiter activates READY- and allows that th microprocessor can complete the current instruction and accept the T flag.
The TOEN is the signal that enable (HIGH) the time out error circutry When LOW, it resets the TO signal and disables the logic.

8 INTERRUPT CONTROL LOGIC.

The arbiter can operate in an E-BUS interrupt mode as well. When interrupt source wants to send a vector interrupt it activates (LOW) th interrupt request input (IRQI-). The arbiter drives the GRANTOUT to LO and waits for the bus to be free via GRANTIN and BUSYIN- (see apendix fig. 4). If it finds the bus free it generates for one BCLK cycle a interrupt enable (INTE-) signal. This signal serves also to activate th buffer, which puts the interrupt vector on to the E-BUS. If there is n response from the microprocessor which handles the interrupt, the vectc is sent again after a 128 BCLK cycles as long as the IRQI- input i active.
The interrupt arbitration request through IRQI- has a higher on-chi priority than the BRQ- request. This means that the arbiter will inhibi a bus transfer (BEN goes LOW) at the end of a cycle (CYEND = LOW) for or BCLK cycle to issue an interrupt if no higher priority device i requesting the bus and the LOCK- input is inactive (see also appendix fig. 4).

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9 SYSTEM CONFIGURATIONS.

Some Applications of the SN74LSXXX Bus Arbiter/E-Bus Interrupt Controll
are presented in appendix B.

10 PIN ASSIGNMENTS.

Figure 4 shows the arbiter 20 pin DIL package. All signals are describ
on the following pages.

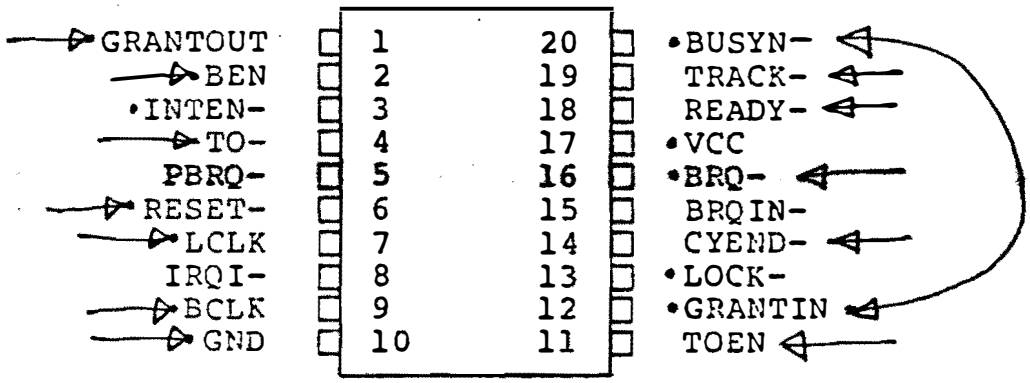

Figure 4: 20 pin dual in line package

→ INDICATES USED ON CORTEX

↷ " OPPOSITE ON CORTEX.

GNATURE	I/O	DESCRIPTION
RESET-	IN	RESET: RESET- is an active LOW signal input which is used to RESET/Initialize the arbiter. After RESET no arbiter has the bus and all output signals are inactive.
LCLK	IN	LOCAL CLOCK: This is the on board clock which serves to synchronize the release logic so that the bus can be surrendered with proper timing. It is also used as the time out clock and to synchronize READY-.
BCLK	IN	BUS CLOCK: The multi master system clock which synchronizes bus arbitration.
BRQ-	IN	BUS REQUEST: BRQ- is an active LOW input signal which tells the arbiter to request the bus by pulling GRANTOUT LOW and activating PBREQ-, and to occupy it as long as no higher priority bus master request is received.
IRQI-	IN	INTERRUPT REQUEST IN: This input is an active LOW signal, which serves to generate an E-BUS interrupt cycle every 128 BCLK cycles as long as IRQI- stays active.
PBRQ-	OUT	PARALLEL BUS REQUEST: This active LOW output serves as a parallel bus request and is activated by the arbiter to indicate an access request. It will stay active as long as BRQ- is active, an interrupt cycle is pending, and the arbiter is not the current bus master.
INTE-	OUT	INTERRUPT ENABLE: INTE- is driven active LOW for one BCLK cycle if the arbiter has the bus and is generating an E-BUS interrupt cycle.
BRQIN-	IN	BUS REQUEST INPUT: BRQIN- is an input signal to the arbiter which serves to indicate if a lower priority master is requesting access to the bus. The BRQIN- is connected to a bidirectional bus line driven by the GRANTOUT signal of all arbiters in the system. If the BRQIN- input is active and the arbiter is the current bus master without an active bus request through BRQ- or IRQI- it will release the bus to the lower priority master.

GRANTIN	IN	ACCESS GRANT IN: This is an input signal that, when HIGH, indicates to a potential bus master that no higher priority bus master device requires access to the bus, and consequently allows it to vie for contr of the bus.
GRANTOUT	OUT	ACCESS GRANT OUT: When HIGH, it indicates that lower priority bus masters may vie for control of the bus. This signal is used in the serial priority resolving scheme. The GRANTOUT pin of one slot is always connected to the GRANTIN pin of the next slot with lower positional priority. GRANTOUT will go active (LOW), sychronized with BCLK, after a bus or interrupt request has arrived. It will go i active, when the device has acquired the bu
LOCK-	IN	LOCK: LOCK- is an active used to inhibit the arbiter from surrenderi the bus to any other bus master requesting access (regardless of priority). It will al inhibit any interrupt cycle request through IRQI-.
BEN	OUT	BUS ENABLE: BEN is an active HIGH output an serves to signal a bus controller, the bus transceiver, and any other devices, that th system bus can be connected to the local bu BEN is also used to drive the BUSY- bus li through an open collector bus driver (activ LOW) to indicate to all other possible bus masters that the bus is occupied.
BUSYIN-	IN	BUSY IN: BUSYIN- is an active LOW input fro the system bus and indicates that the bus is currently used by another bus master. A HIGH level on BUSYIN- and GRANTIN signals the arbiter that the bus is not used and can be occupied after the LOW to HIGH transition of BCLK.
TRACK-	IN	TRANSFER ACKNOWLEDGE: TRACK- is an input signal, when active (LOW), indicates that a addressed slave device is ready to complete its read or write operation. This signal is synchronized with the raising edge of LCLK and fed to the READY- output.

READY-	OUT	READY: READY- is an output signal which, when active (LOW), indicates to the microprocessor that it can complete its read or write operation. READY- is synchron to the LCLK. READY- is the same as the TRACK- signal on normal operation. It will be internally created in the time out mode (TOEN=HIGH) when a TIME OUT error is detected.
CYEND-	IN	CYLE END: CYEND- is a signal generated by the microprocessor which, when active (LOW), allows the arbiter to surrender the bus if a higher priority master requests the bus via GRANTIN.
TO-	OUT	TIME OUT: TO- is an active LOW output signal which is used to flag the microprocessor that a time out error is detected on the bus. The signal is generated only when TOEN is active.
TOEN	IN	TIME OUT ENABLE: TOEN is an input signal (active HIGH) which enables the TIME OUT CONDITION DETECTION scheme to create a TO flag and READY- signal in two cases: a) When the arbiter does not get the bus for 128 BCLK cycles. b) When the arbiter has acquired the multi master bus, an input or output operation has been initiated, and no response is received after 16 LCLK cyles from the addressed slave device. This scheme is a guard against bus errors and bus dead locks. When TOEN does go LOW, it ar clears the TO error flag and disables the time out logic.
VCC	IN	Supply voltage +5 volts DC +/-5%.
GND	IN	Ground.

11 ELECTRICAL SPECIFICATIONS.

11.1 RECOMMANDED OPERATING CONDITIONS.

PARAMETER	MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}	4,75	5	5,25	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0,8	V
Operating free-air temperature, T_A		0	70	°C

11.2 ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMANDED. OPERATING CONDITIONS (UNLESS OTHERWISE NOTED).

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_I	Input current at max. input voltage	V_{CC} = max, V_{IH} = 7V				0.1	µA
I_{OL}	Low-level output current						
	READY- signal *	V_{OL} = 0.5V				16	mA
	GRANTOUT signal *	V_{OL} = 0.4V				8	mA
	PBRQ- signal	V_{OL} = 0.5V				8	mA
	INTE- signal	V_{OL} = 0.4V				8	mA
	BEN signal	V_{OL} = 0.4V				8	mA
	TO- signal	V_{OL} = 0.4V				8	mA
I_{OH}	High-level output current	V_{OH} = 2.7V				* -400	µA
I_{OH}	High-level output current *	V_{OH} = 2.7V				-250	µA
I_{IH}	High-level input current	V_{CC} = max, V_{IH} = 2.7V				20	µA
I_{IL}	Low-level input current, GRANTIN	V_{CC} = max, V_{IL} = 0.5V				-0.4	mA
I_{IL}	Low-level input current, all others	V_{CC} = max, V_{IL} = 0.5V				-0.2	mA
V_{OL}	Low-level output voltage	V_{CC} = min, V_{IH} = 2V, V_{IL} = V_{ILmax}	I_{OL} = 8mA			0.4	V
			I_{OL} = 16mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = min, V_{IH} = 2V, V_{IL} = V_{ILmax}, I_{OH} = -400µA		2.7	3.4		V
I_{CC}	Supply current	V_{CC} = max			60		mA

* Open collector output with 10K ohm pull up

11.3 TIMING REQUIREMENTS OVER FULL RANGE OF OPERATING CONDITIONS.

	PARAMETER	MIN	TYP	MAX	UNIT
T_{BCLK}	Bus clock cycle time	100	250		ns
T_{BCLK} R	Bus clock rise time		10	15	ns
T_{BCLK} F	Bus clock fall time		10	15	ns
T_{BCLK} W(L)	Bus clock pulse width (low-level)	50	125		ns
T_{BCLK} W(H)	Bus clock pulse width (high-level)	50	125		ns
T_{LCLK}	Local clock cycle time	100	250		ns
T_{LCLK} R	Local clock rise time		8	10	ns
T_{LCLK} F	Local clock fall time		8	10	ns
T_{LCLK} W(L)	Local clock pulse width (low-level)	50	125		ns
T_{LCLK} W(H)	Local clock pulse width (high-level)	50	125		ns
T_R W(L)	Reset pulse width (low-level)		50		ns

11.4 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMANDED OPERATING CONDITIONS.

	PARAMETER	MIN	TYP*	MAX*	UNIT
T_{SB}	Setup time BUSYIN- before BCLK↑		15	20	ns
T_{HB}	Hold time BUSYIN- after BCLK↑	0	20		ns
T_{dBEH}	Delay time BEN (high) after BCLK↑		10		ns
T_{dBEL}	Delay time for BEN after LCLK↓		10		ns
T_{dGO}	Delay time GRANTOUT after BCLK↑	0	10		ns
T_{SBRIN}	Setup time BRQIN-		20		ns
T_{HBRIN}	Hold time in BRQIN-	0			ns
T_{dPBRL}	Delay time PBRQ- (low) after BCLK↑		20		ns
T_{dPBRH}	Delay time PBRQ- (high) after LCLK		20		ns
T_{dIT}	Delay time INTE- after BCLK↑		10		ns
T_{SGI}	Setup time before BCLK↑		10		ns
T_{HGI}	Hold time GRANTIN after BCLK↑	0			ns
T_{STR}	Setup time TRACK- before LCLK↑		10		ns
T_{dRH}	Delay time READY- (high) after CYEND- (low)		20		ns
T_{dTRL}	Delay time READY- (low) after LCLK↑		15		ns
T_{dTOL}	Delay time TO- (low) after LCLK↑		20		ns
T_{dTOH}	Delay time TO- (high) after TOEN (low)		20		ns

* design goals

APPENDIX A: TIMING DIAGRAMS

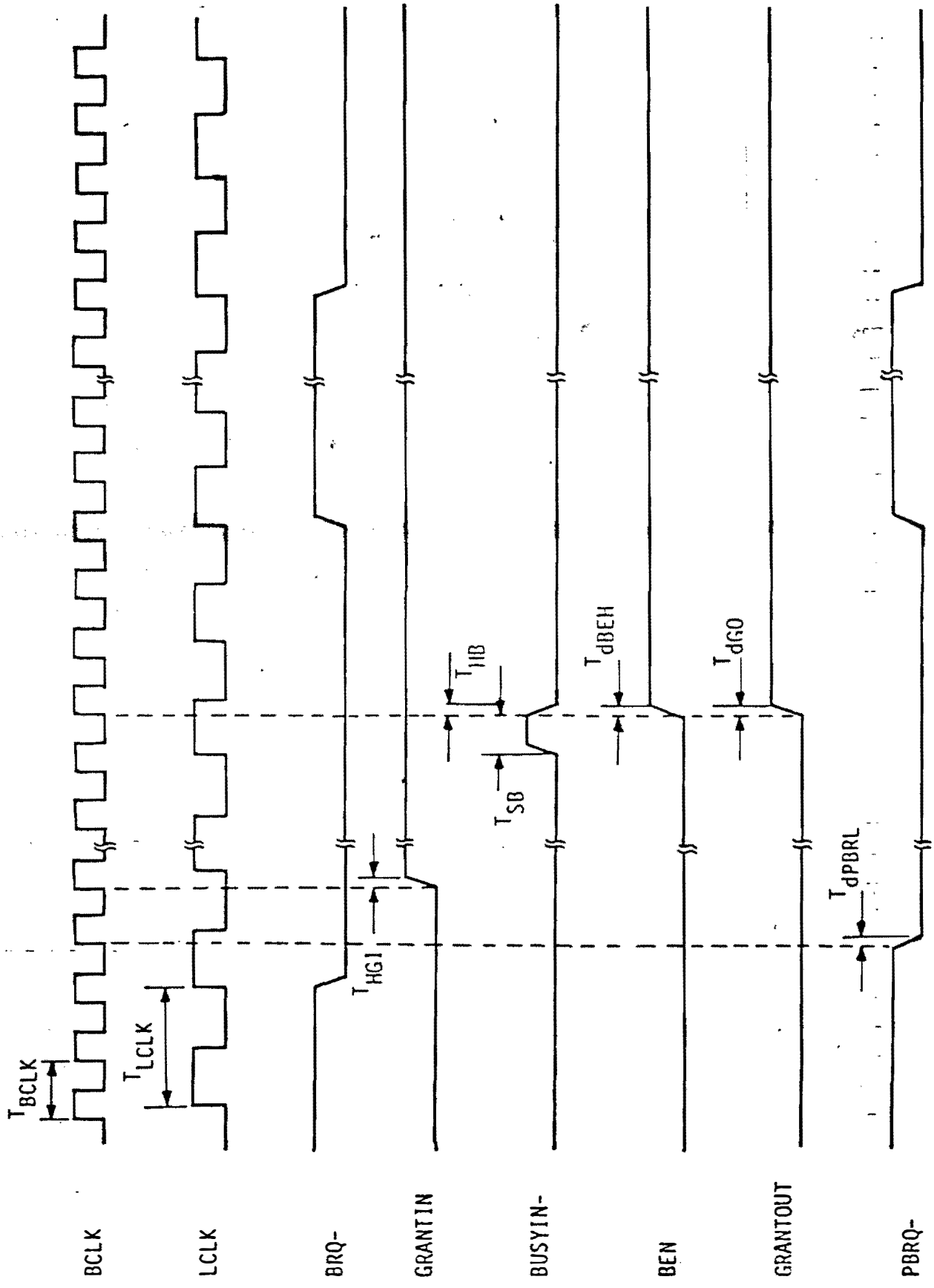

Figure 1: Bus Regests

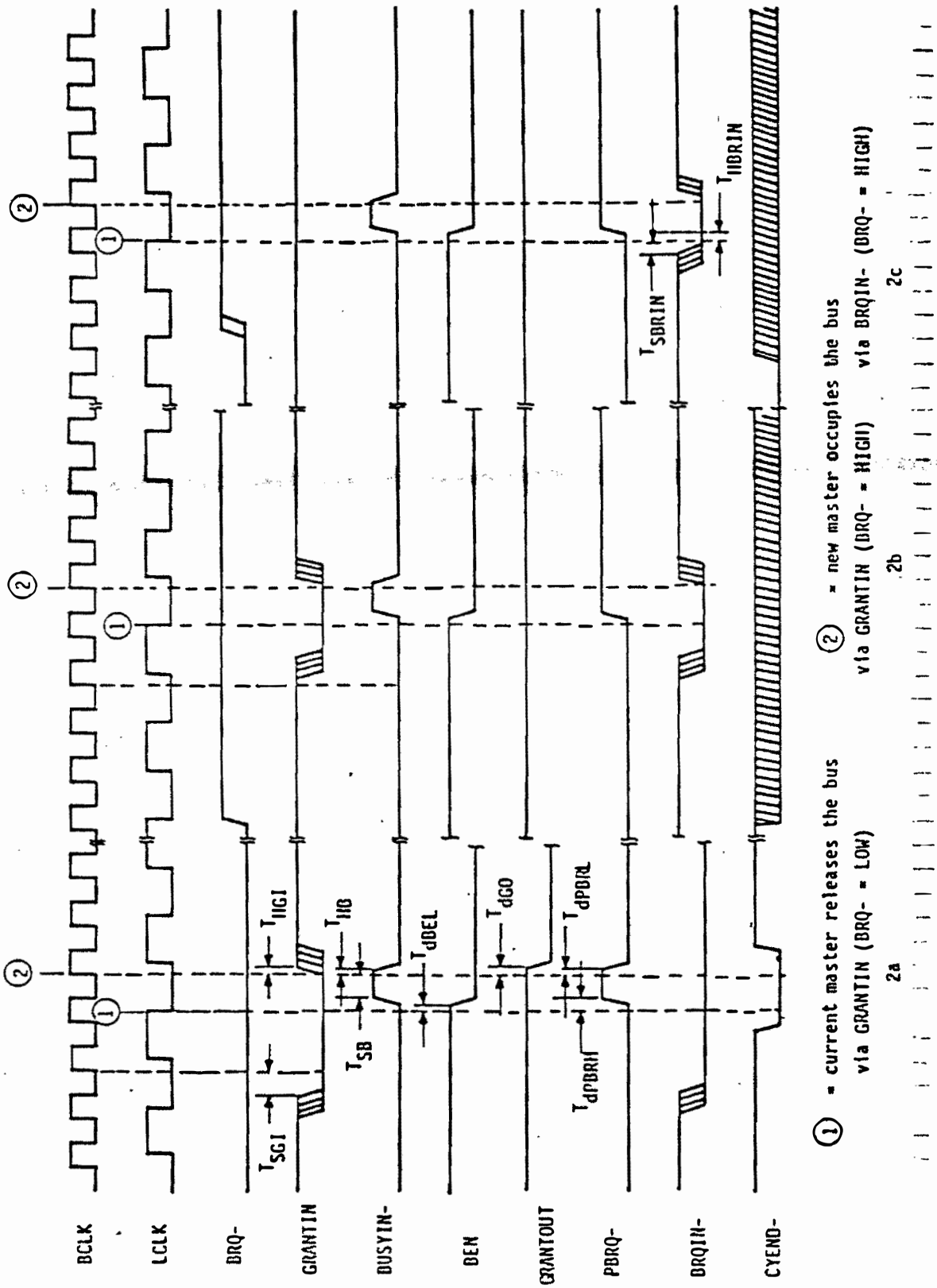

Figure 2: Bus Surrendering

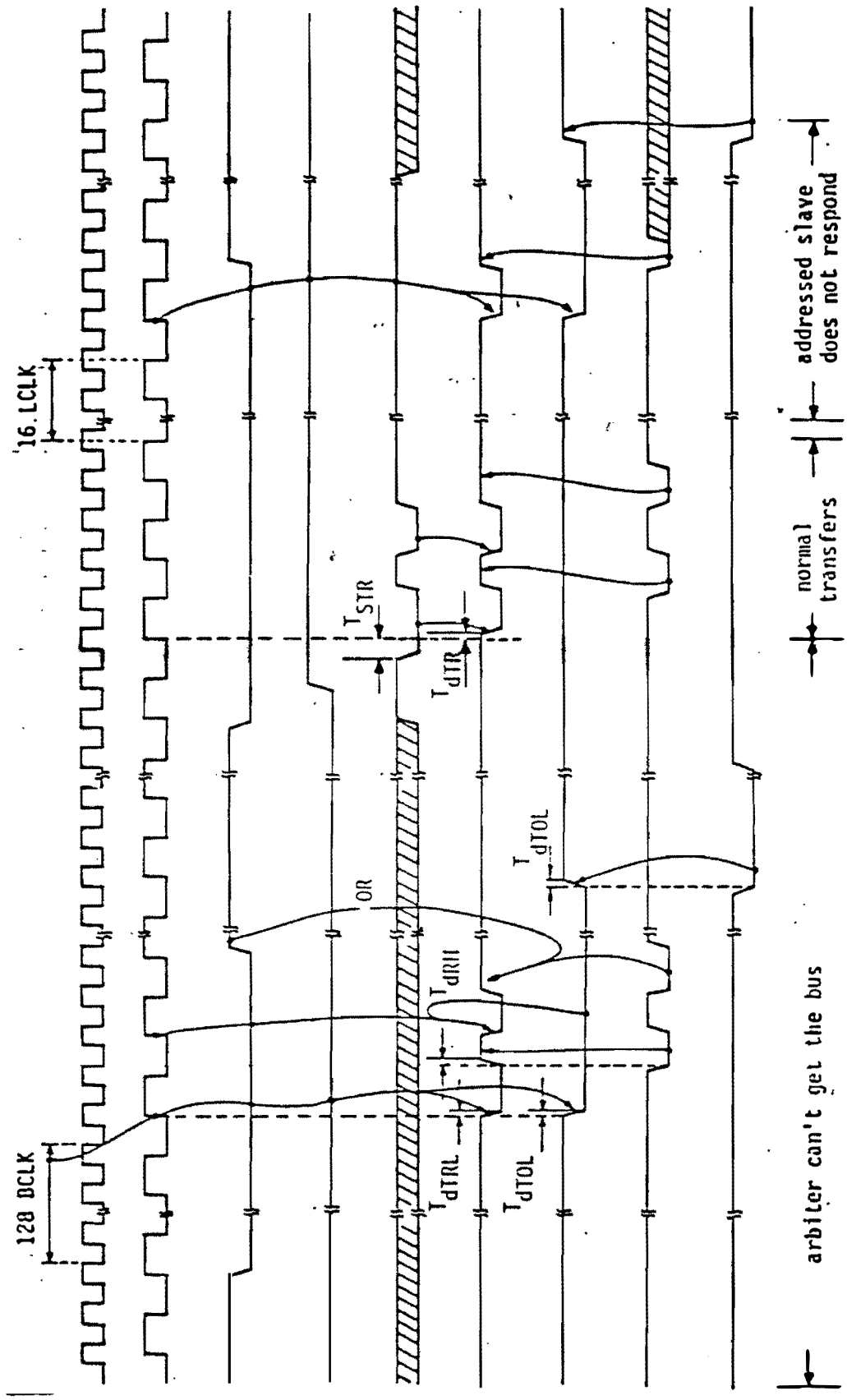

Figure 3: Ready & Bus Anti Dead Lock Logic

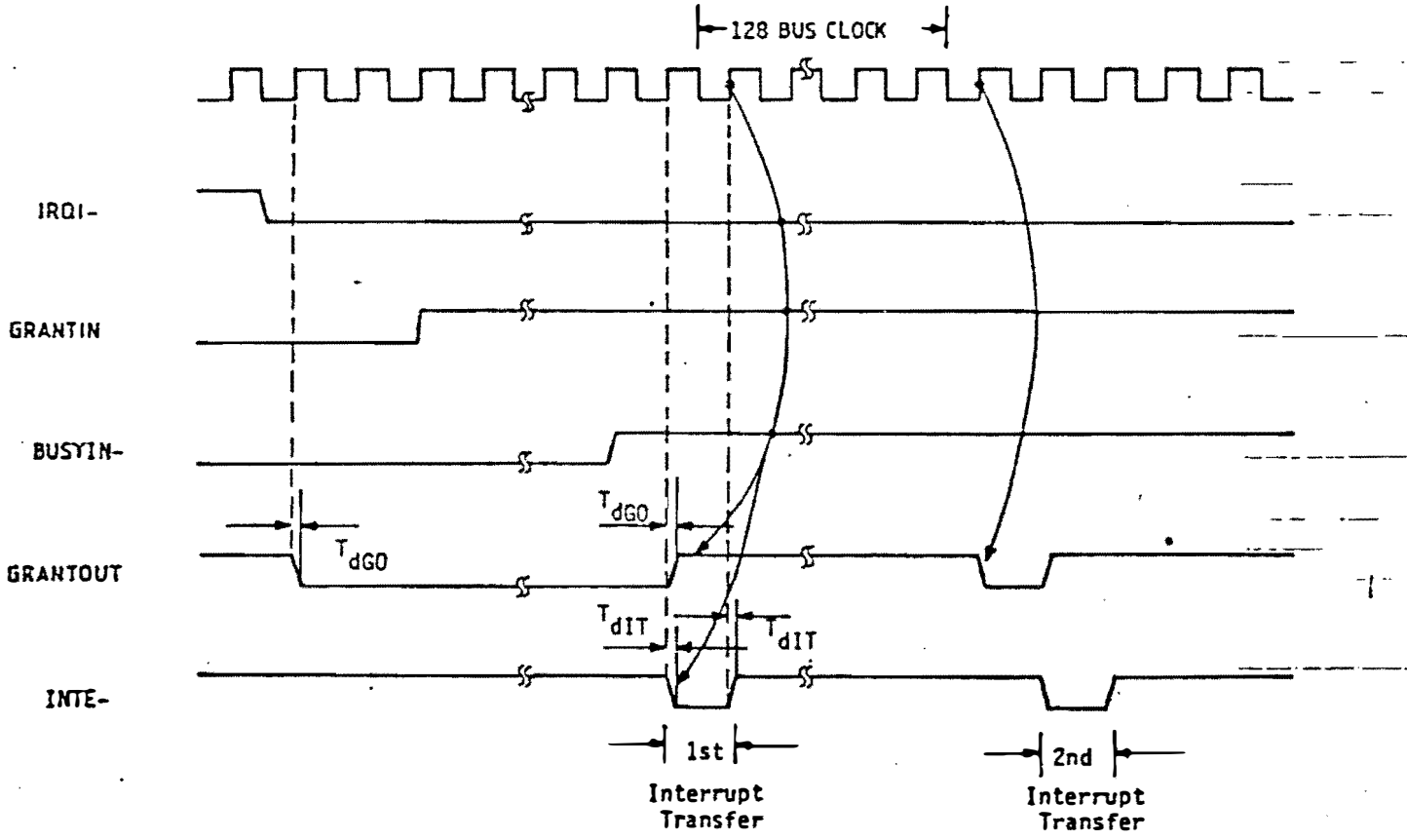

Figure 4: Interrupt Timing

APPENDIX B: SYSTEM CONFIGURATION BLOCK DIAGRAMS

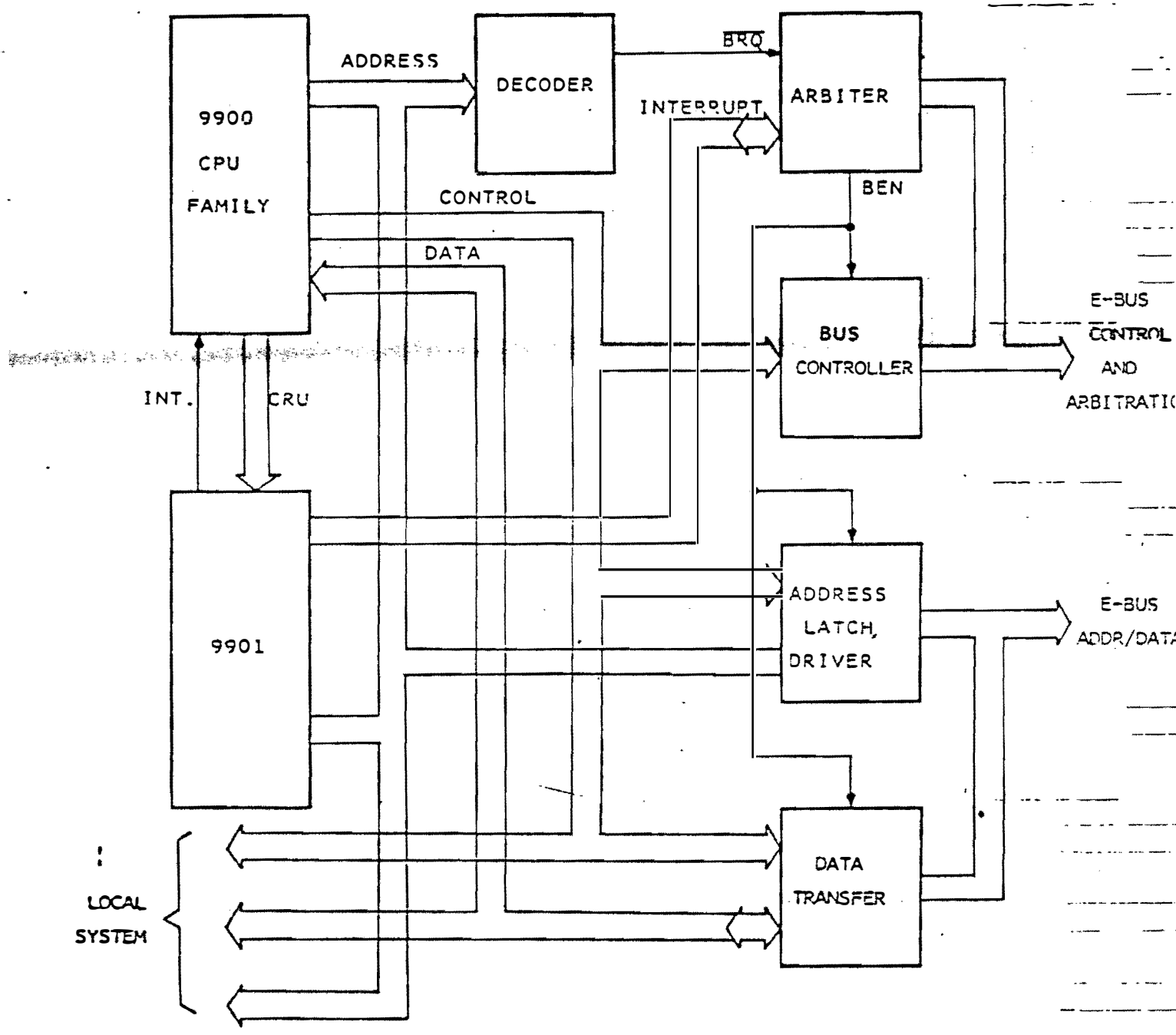

Figure 1: 99XXX Family Multiprocessing

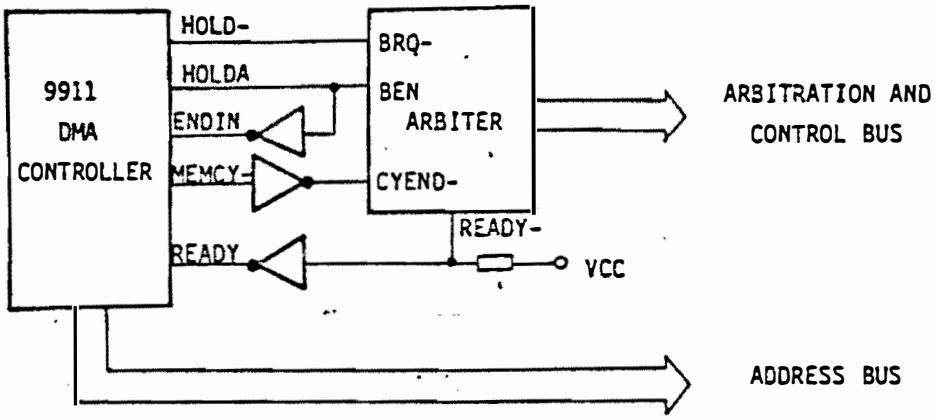

Figure 2: Multiprocessing with TMS 9911 DMA-Controller

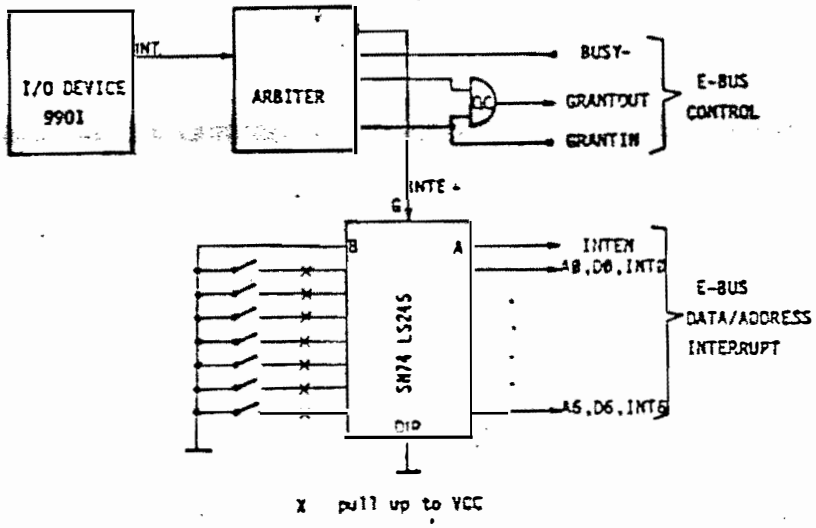

Figure 3: Interrupt Control

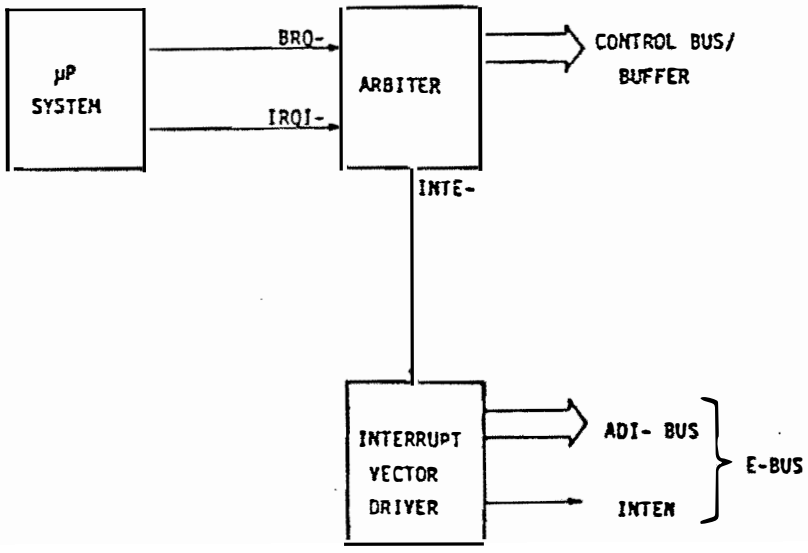

Figure 4: Bus Arbitation & Interrupt Control