Keyboard Encoder

FEATURES

- One integrated circuit required for complete keyboard assembly
- Outputs directly compatible with TTL/DTL or MOS logic arrays
- External control provided for output polarity selection
- External control provided for selection of odd or even parity
- Two key roll-over operation
- N-key lockout
- Programmable coding with a single mask change
- Self-contained oscillator circuit
- Externally controlled delay network provided to eliminate the effect of contact bounce
- Static charge protection on all input and output terminals
- Entire circuit protected by a layer of glass passivation

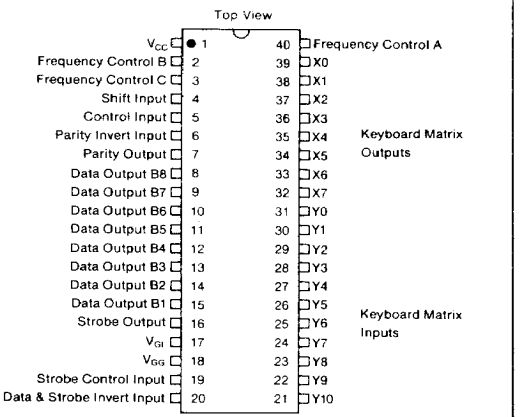
DESCRIPTION

The General Instrument AY-5-2376 is a 2376 Bit Read Only Memory with all the logic necessary to encode single pole single throw keyboard closures into a usable 9-bit code. Data and strobe outputs are directly compatible with TTL/DTL or MOS logic arrays without the use of any special interface components.

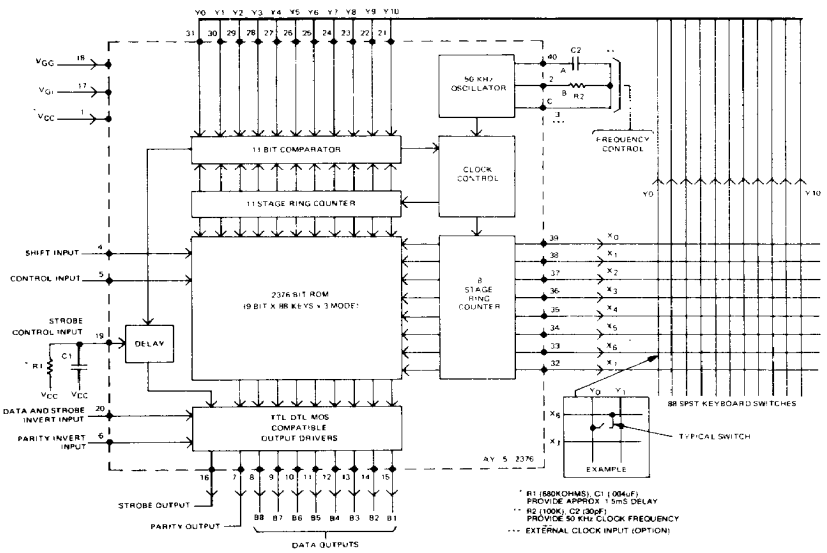
The AY-5-2376 is fabricated with MTNS technology and contains 2942 P-channel enhancement mode transistors on a single monolithic chip.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



OPERATION

The AY-5-2376 contains (see Block Diagram) a 2376-bit ROM, 8-stage and 11-stage ring counters, an 11-bit comparator, an oscillator circuit, an externally controllable delay network for eliminating the effect of contact bounce, and TTL/DTL/MOS compatible output drivers.

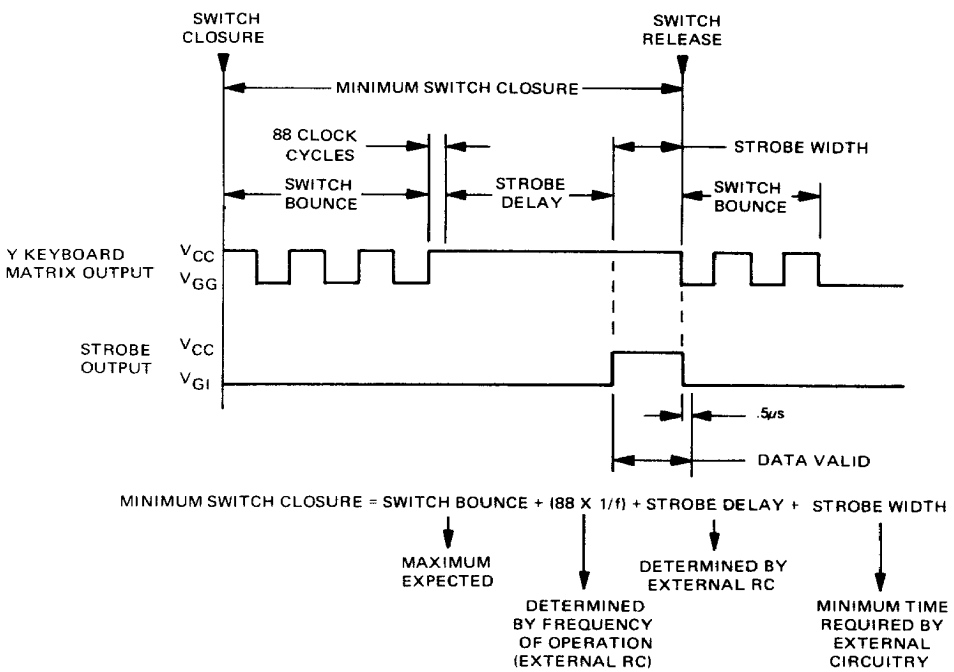
The ROM portion of the chip is a 264 by 9 bit memory arranged into three 88-word by 9-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the three 88-word groups; the 88-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

The external outputs of the 8-stage ring counter and the external inputs to the 11-bit comparator are wired to the keyboard to form an X-Y matrix with the 88-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM; the absence of a Strobe Output indicates that the Data Outputs are 'not valid' at this time.

When a key is depressed, a single path is completed between one output of the 8-stage ring counter (X0 thru X7) and one input of the 11-bit comparator (Y0-Y10). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 11-stage ring counter. When this occurs, the comparator generates a signal to the clock control and 9, the Strobe Output (via the delay network). The clock control stops the clocks to the ring counters and the Data Outputs (B1-B9) stabilize with the selected 9-bit code, indicated by a 'valid' signal on the Strobe Output. The Data Outputs remain stable until the key is released.

As an added feature two inputs are provided for external polarity control of the Data Outputs. Parity Invert (pin 6) provides polarity control of the Parity Output (pin 7) while the Data and Strobe Invert Input (pin 20) provides for polarity control of Data Outputs B1 thru B8 (pins 8 thru 15) and the Strobe Output (pin 16).

TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings

V_{GI} and V_{GG} (with respect to V_{CC}) . . . . . −20V to +0.3V
Logic input voltages (with respect to V_{CC}) . . . −20V to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

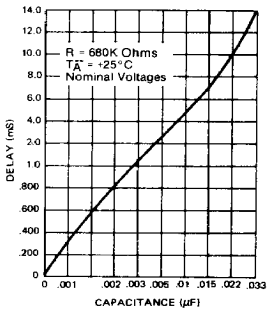
V_{CC} = +5 Volts ± 0.5 Volts, (V_{CC} = Substrate Voltage)
V_{GG} = −12 Volts ± 1.0 Volts, V_{GI} = GND. Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
Clock Frequency	f	10	50	100	KHz	See Block diagram footnote** for typical R - C values
Data Input (Shift, Control, Parity invert, data & strobe invert).						
Logic "0" Level	V_{I0}	V_{GG}	—	+0.8	V	
Logic "1" Level	V_{I1}	V_{CC}−1.5	—	V_{CC}+0.3	V	
			—			
Shift & Control Input Current	$I_{INS,C}$	15	36	60	μA	V_I=+5V
		8	16	30	μA	V_I= 0V
Data, Parity Invert Input Current	$I_{IND,P}$	—	.01	1	μA	V_I=−5V to +5V
X Output (X_0-X_7)						
Logic "1" Output Current	I_{XI}	—	0	—	μA	V_{OUT} = V_{CC}
		80	150	400	μA	V_{OUT} = V_{CC} −1.3V
		140	300	800	μA	V_{OUT} = V_{CC} −2.0V
		250	700	1500	μA	V_{OUT} = V_{CC} −5V
		500	1500	3000	μA	V_{OUT} = V_{CC} — 10V
Logic "0" Output Current	I_{XO}	15	30	80	μA	V_{OUT} = V_{CC}
		13	27	65	μA	V_{OUT} = V_{CC} −1.3V
		12	25	60	μA	V_{OUT} = V_{CC} −2.0V
		5	10	40	μA	V_{OUT} = V_{CC} −5V
		—	1	20	μA	V_{OUT} = V_{CC} −10V
Y Input (Y_0-Y_{10})						
Trip Level	V_Y	V_{CC} −5	V_{CC} −3	V_{CC}−2	V	Y Input Going Positive
Hysteresis	ΔV_Y	.5	.9	1.4	V	Note 1
						Note 2
Selected Y Input Current	I_{YS}	30	60	160	μA	V_{IN} = V_{CC}
		26	54	130	μA	V_{IN} = V_{CC} −1.3V
		24	50	120	μA	V_{IN} = V_{CC} −2.0V
		10	20	80	μA	V_{IN} = V_{CC} −5V
		—	2	20	μA	V_{IN} = V_{CC} −10V
Unselected Y Input Current	I_{YU}	15	30	80	μA	V_{IN} = V_{CC}
		13	27	65	μA	V_{IN} = V_{CC} −1.3V
		12	25	60	μA	V_{IN} = V_{CC} −2.0V
		5	10	40	μA	V_{IN} = V_{CC} −10V
Input Capacitance	C_{IN}	—	3	10	pF	at 0V
Switch Characteristics						
Minimum Switch Closure Contact Closure Resistance	—	—	—	—	—	See Timing Diagram
	Z_{CC}	—	—	300	Ω	
	Z_{CO}	1×10⁷	—	—	Ω	
Strobe Delay						
Trip Level (Pin 19)	V_{SD}	V_{CC}−4	V_{CC}−3	V_{CC}−2	V	
Hysteresis	V_{SD}	.5	.9	1.4	V	See Note 1
Quiescent Voltage (Pin 19)		−3	−5	−8	V	With 680K to V_{SS}
Data Output (B_1-B_8)						
Logic "0"	—	—	—	0.4	V	I_{OL} = 1.6ma
Logic "1"	—	V_{CC}−1	—	—	V	I_{OH}−100μa
Power						
I_{CC}	—	—	5	10	mA	V_{CC} = +5V
I_{GG}	—	—	5	10	mA	V_{GG} = −12V

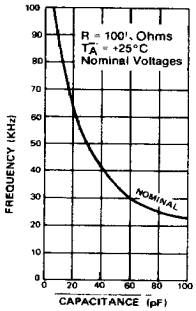
**Typical values at +25°C and nominal voltages.

NOTE 1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Guaranteed number of X & Y loads which may be applied to an X output = eleven.

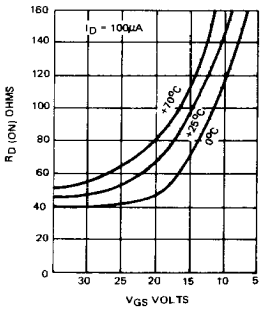
TYPICAL CHARACTERISTIC CURVES



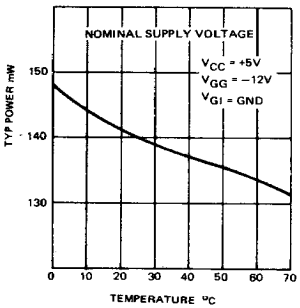
STROBE DELAY C1



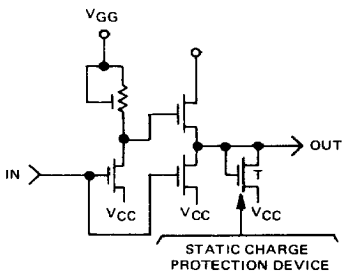
OSCILLATOR FREQUENCY VS. C2



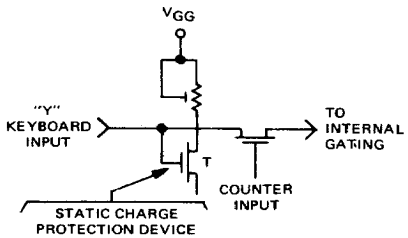
TYPICAL OUTPUT ON RESISTANCE (R_{DON}) VS. GATE BIAS VOLTAGE (V_{GS})



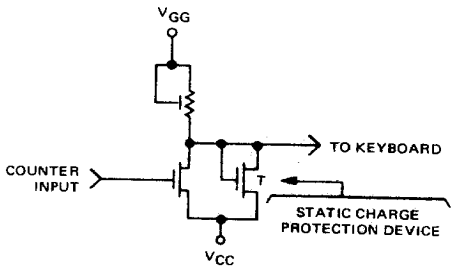
TYPICAL POWER CONSUMPTION (mW) VS. TEMP (°C)



OUTPUT DRIVER

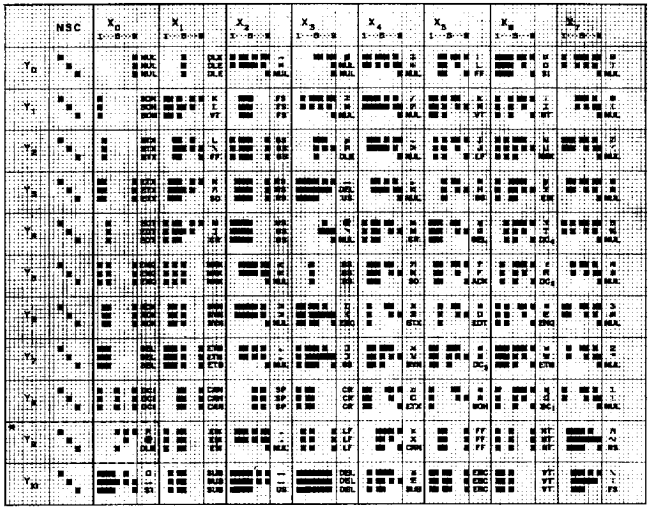


"Y" INPUT STAGE FROM KEYBOARD



"X" OUTPUT STAGE TO KEYBOARD

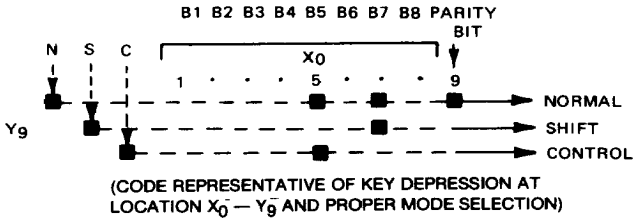
STANDARD CODE ASSIGNMENT CHART



Illustrated using a Logic "O" on the Data and Strobe Invert Input (Pin 20) and the Parity Invert Input (Pin 6).

NOTE 1: This code is an 8 bit ASCII code (B1-B8). Output B9 is included as an odd parity bit operating on outputs B1-B7.

*EXAMPLE



(CODE REPRESENTATIVE OF KEY DEPRESSION AT LOCATION X_0^- — Y_9^- AND PROPER MODE SELECTION)

N = NORMAL MODE
S = SHIFT MODE
C = CONTROL MODE
■ = OUTPUT LOGIC "1" (SEE DATA B1 – B8)
LOGIC "1" = +5V
LOGIC "0" = GND

TRUTH TABLES

DATA (B1-B8) INVERT TRUTH TABLE

DATA AND STROBE INVERT INPUT (PIN 20)	CODE ASSIGNMENT CHART	DATA OUTPUTS (B1-B8)
1	1	0
0	1	1
1	0	1
0	0	0

PARITY INVERT TRUTH TABLE

PARITY INVERT INPUT (PIN 6)	CODE ASSIGNMENT CHART	PARITY OUTPUT (PIN 7)
1	1	0
0	1	1
1	0	1
0	0	0

STROBE INVERT TRUTH TABLE

DATA AND STROBE INVERT INPUT (PIN 20)	INTERNAL STROBE	STROBE OUTPUT (PIN 16)
1	1	0
0	0	0
1	0	1
0	1	1

MODE SELECTION

$\overline{S}$ $\overline{C}$ = N
$\overline{S}$ C = S
S $\overline{C}$ = C
S C = C